CMS32L051 datasheet

ARM® Cortex®-M0+ based, ultra low power consumption 32-bit microcontroller

Built-in 64K byte Flash, rich simulation function, timer and various communication interfaces

V1.80

Features

- **Ultra-low power consumption operating environment:**
  - Power supply voltage range: 1.8V to 5.5V
  - Temperature range: -40℃ to 105℃
  - Low power consumption mode: sleep mode, deep sleep mode
  - Operating power consumption: 70uA/MHz@64MHz
  - Power consumption in deep sleep mode:80uA
  - Power consumption in deep sleep mode with partial power failure: 4.5uA
  - Deep sleep mode with partial power failure +32.768K+RTC: 5uA
- **Core:**
  - ARM®32-bitCortex®-M0+ CPU
  - Working frequency: 32KHz～64MHz
- **Memory:**
  - 64KB Flash memory, with program and data storage shared
  - 1.5KB dedicated data Flash memory
  - 8KB SRAM memory with parity check
- **Power and reset management:**
  - Built-in power-on reset (POR) circuit
  - Built-in voltage detection (LVD) circuit (threshold voltage can be set)
- **Clock management:**
  - Built-in high-speed vibrator, accuracy (±1%) .Can provide 2MHz～64MHz system clock and peripheral module operation clock
  - Built-in 15KHz low-speed oscillator
  - Support 1MHz～20MHz external crystal oscillator
  - Support 32.768KHz external crystal oscillator, can be used to calibrate the internal high-speed vibrator
- **Multiplier module:**
  - Support single cycle 32bit multiplication operation
- **Enhanced DMA controller:**
  - Interrupt trigger start.
  - Transmission mode is selectable (normal transmission mode, repeated transmission mode, block transmission mode and chain transmission mode)
- **Analog peripheral:**
  - 12-bit precision ADC converter, conversion rate 500Ksps, 35 external analog channels, internal optional PGA0 output as conversion channel, with temperature sensor, support single-channel conversion mode and multi-channel scan conversion mode Conversion range: 0 to positive reference voltage
- **Input/output port:**
  - Number of I/O port: 16～45
  - Can switch between N-channel open drain and internal pull-up and pull-down
  - Built-in button interrupt detection function
  - Built-in clock output/buzzer output control circuit
- **Serial two-wire debugger (SWD)**
- **Abundant timer:**
  - 16-bit timer: 8 channels
  - 15-bit interval timer: 1
  - Real-time clock (RTC): 1 (with perpetual calendar, alarm clock function, and supports a wide range of clock correction)
  - Watchdog timer (WWDT): 1
  - SysTick timer
- **Abundant and flexible interface:**
  - 3-channel serial communication unit: each channel can be freely configured as a 1-channel standard UART, 2-channel SPI or 2-channel simple I2C
  - Standard SPI: 1 channel (support 8bit and16bit)
  - Standard I2C: 1 channel
  - IrDA: 1 channel
- **security function:**
  - Comply with relevant standards of IEC/UL 60730
  - Abnormal storage space access error
  - Support RAM parity check
  - Support hardware CRC check
  - Support important SFR protection to prevent misoperation
  - 128-bit unique ID number
  - d Flash secondary protection in debug mode (level1: only the entire flash area can be erased, not read or write; level2: the emulator connection is invalid, and the flash operation is not possible)

- The transmission source/destination area is optional for the full address space range

- **Linkage controller:**
  - The event signals can be linked together to realize the linkage of peripheral functions.
  - 15 types of event input, 4 types of event trigger.

- **Encapsulation:**
  - Support multiple encapsulation of 20 Pin to 48 Pin

1 Overview

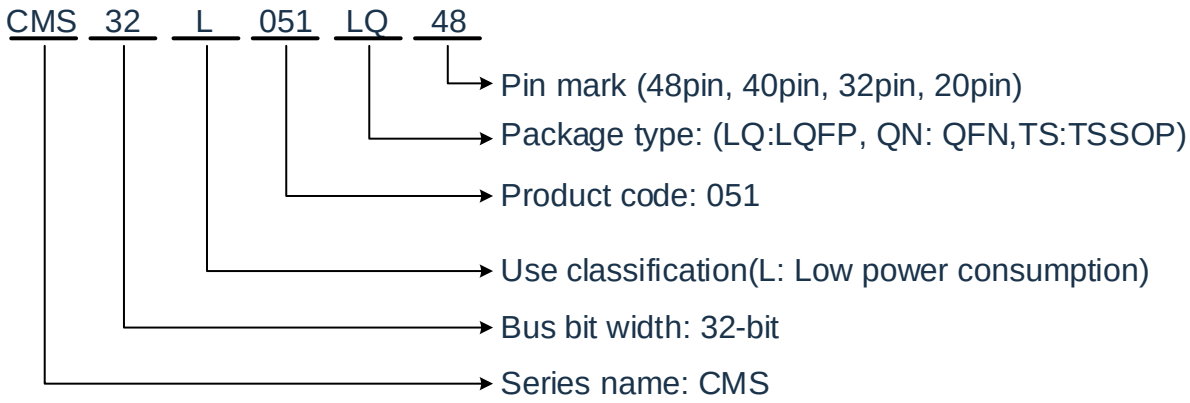
1.1 Introduction

Ultra-low power consumption CMS32L051 uses high-performance 32-bit RISC core of ARM®Cortex®-M0+, can work at a frequency of up to 64 MHz, and adopts high-speed embedded flash memory (SRAM max. 8KB, program/data flash memory max. 64KB) This product integrates multiple standard interfaces of I2C, SPI, UARTand LIN Integrated 12bit A/D converter, temperature sensor. Among them, the 12bit A/D converter can collect external sensor signals, reducing system design costs. The temperature sensor integrated in the chip can realize real-time monitoring of the external ambient temperature. Integrated 8-channel 16bit timer module, and equipped with EPWM control circuit, combined with the timer can realize the control of one DC motor or two stepper motors.

CMS32L051 also has excellent low-power performance, supports two low-power modes of sleep and deep sleep, and is designed to be flexible. Its operating power consumption is 70uA/MHz@64MHz, and the power consumption is only 4.5uA in deep sleep mode with partial power-down, which is suitable for battery-powered low-power devices. At the same time, due to the integrated event linkage controller, direct connection between hardware modules can be realized without the intervention of the CPU, which is faster than using interrupt response, while reducing the frequency of CPU activity and prolonging the battery life.

These features make the CMS32L051 microcontroller series can be widely used in consumer civil products, such as household appliances, mobile devices, etc.

1.2 Product model list



List of products of CMS32L051:

Number of Pin	Encapsulation	Product model
20pin	20-pin plastic package TSSOP（6.5X4.4mm，0.65mm pitch）	CMS32L051TS20
20pin	20-pin plastic package QFN（3X3mm, 0.4mm pitch）	CMS32L051QN20
24pin	24-pin plastic package SSOP（8.65X3.9mm, 0.635mm pitch）	CMS32L051SS24
24pin	24-pin plastic package QFN（4X4mm，0.5mm pitch）	CMS32L051QN24
32pin	32-pin plastic package QFN（5X5mm，0.5mm pitch）	CMS32L051QN32
32pin	32-pin plastic package LQFP (7X7mm, 0.8mm pitch)	CMS32L051LQ32
40pin	40-pin plastic packageQFN (5X5mm, 0.4mm pitch)	CMS32L051QN40
48pin	48-pin plastic packageLQFP (7X7mm, 0.5mm pitch)	CMS32L051LQ48

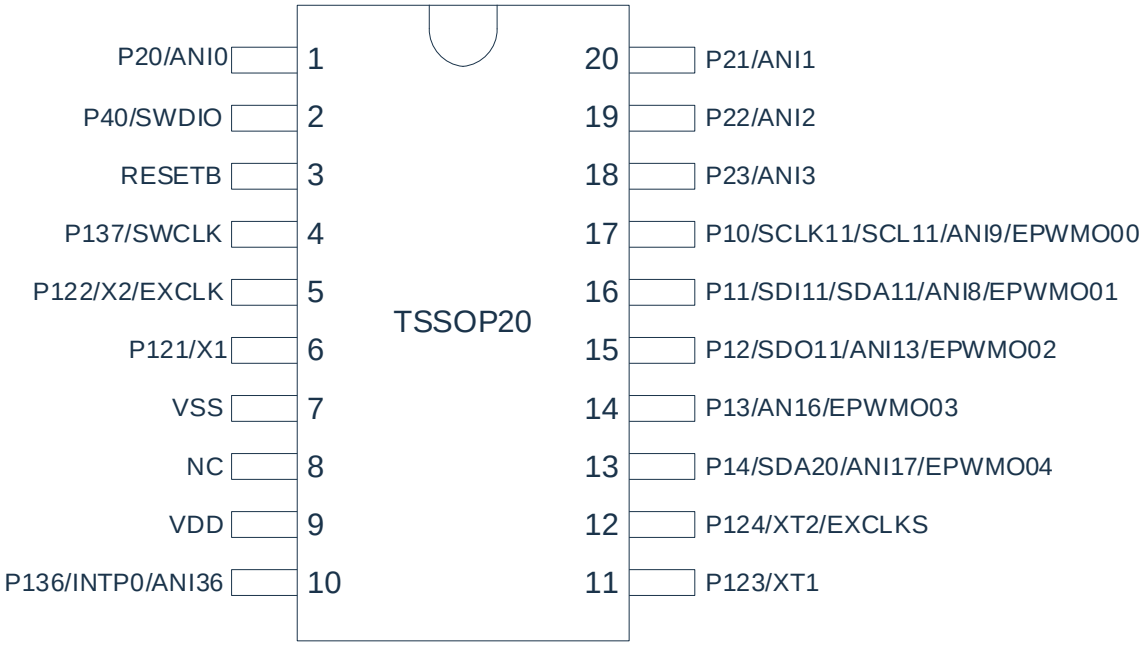
FLASH, SRAM capacity:

Flash memory	Special data Flash memory	SRAM	CMS32L051				
			20pin	24pin	32pin	40pin	48pin
64KB	1.5KB	8KB	CMS32L051TS20 CMS32L051QN20	CMS32L051SS24 CMS32L051QN24	CMS32L051QN32 CMS32L051LQ32	CMS32L051QN40	CMS32L051LQ48

1.3 Pin connection diagram (Top View)

1.3.1 CMS32L051TS20 pin diagram

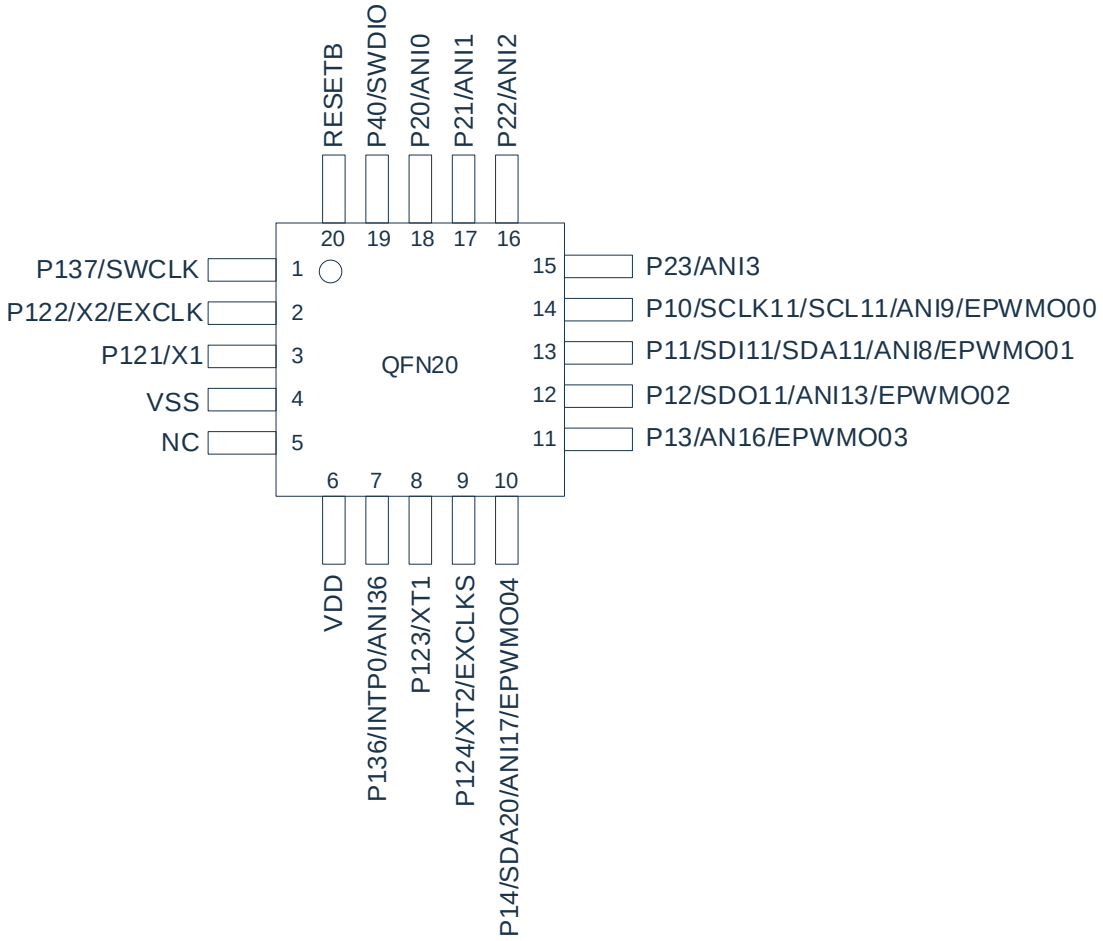
- 20-pin plastic package TSSOP（6.5x4.4mm、0.65mm pitch）



The unmarked digital function support pins in the figure are configurable, see section 4.1 for details

1.3.2 CMS32L051QN20 pin diagram

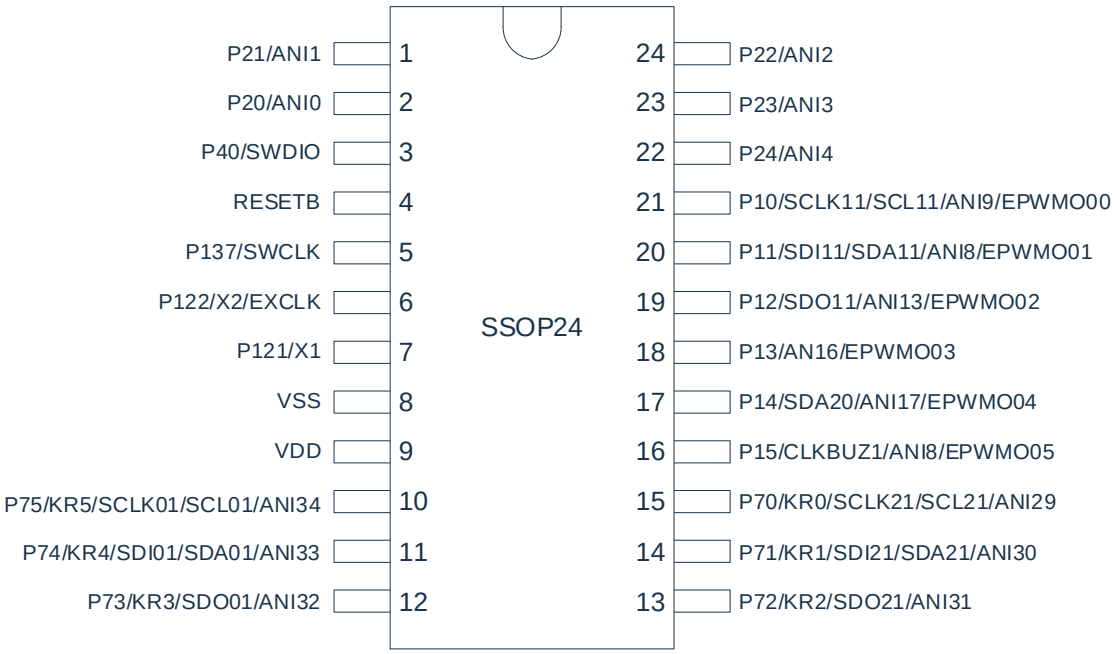
- 20-pin plastic package QFN（3x3mm、0.4mm pitch）



The unmarked digital function support pins in the figure are configurable, see section 4.1 for details

1.3.3 CMS32L051SS24 pin diagram

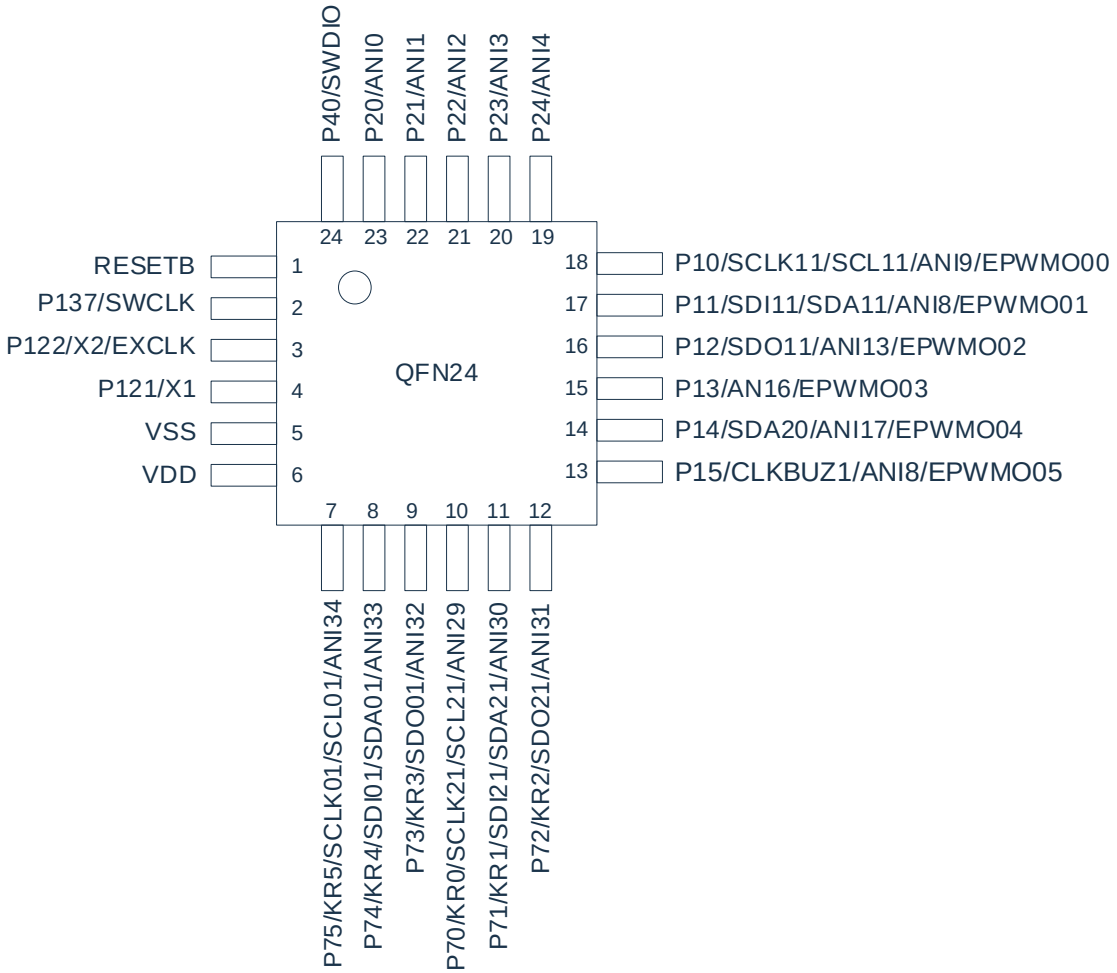
- 24-pin plastic package SSOP（8.65x3.9mm、0.635mm pitch）



The unmarked digital function support pins in the figure are configurable, see section 4.1 for details

1.3.4 CMS32L051QN24 pin diagram

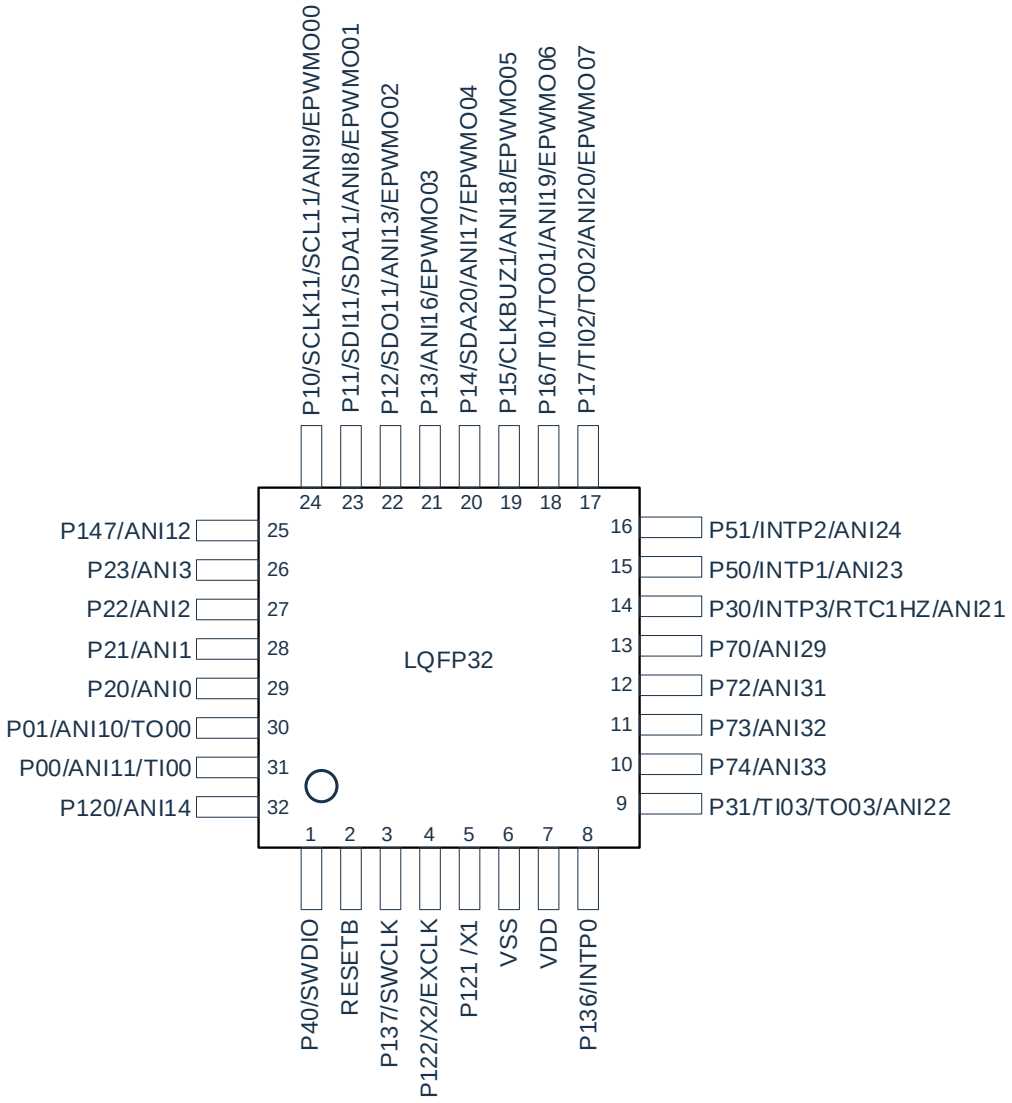
- 24-pin plastic package QFN (4x4mm, 0.5mm pitch)



Note: The unmarked digital function support pins in the figure are configurable, see section 4.1 for details.

1.3.5 CMS32L051LQ32 pin diagram

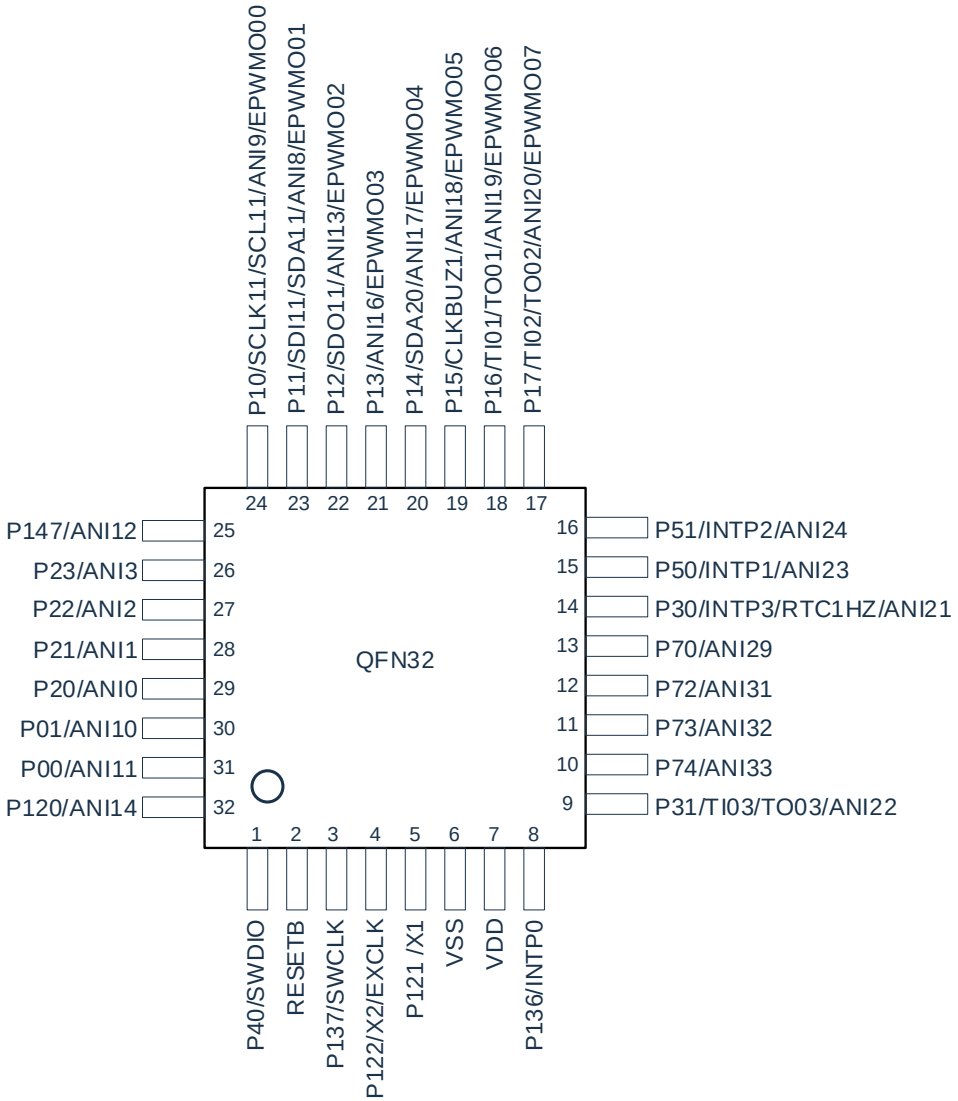
- 32-pin plastic package LQFP（7x7mm、0.8mm pitch）



Note: The unmarked digital function support pins in the figure are configurable, see section 4.1 for details.

1.3.6 CMS32L051QN32 pin diagram

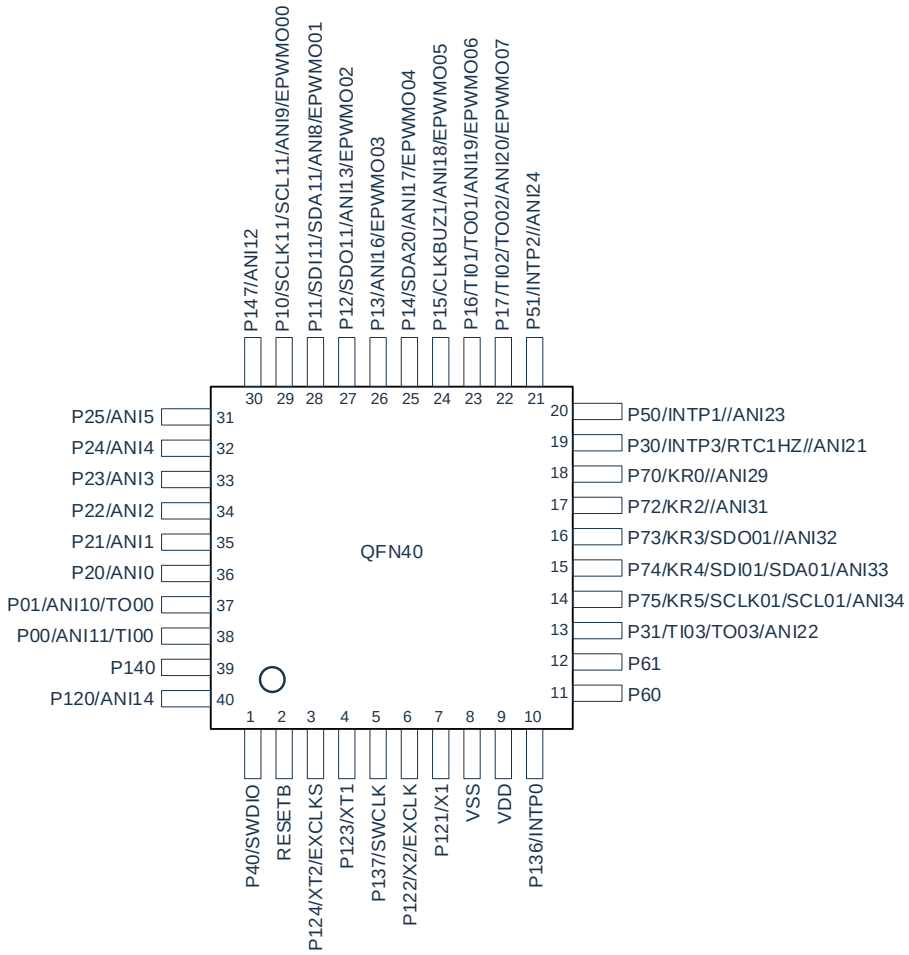
- 32-pin plastic package QFN (5x5mm, 0.5mm pitch)



Note: The unmarked digital function support pins in the figure are configurable, see section 4.1 for details.

1.3.7 CMS32L051QN40 pin diagram

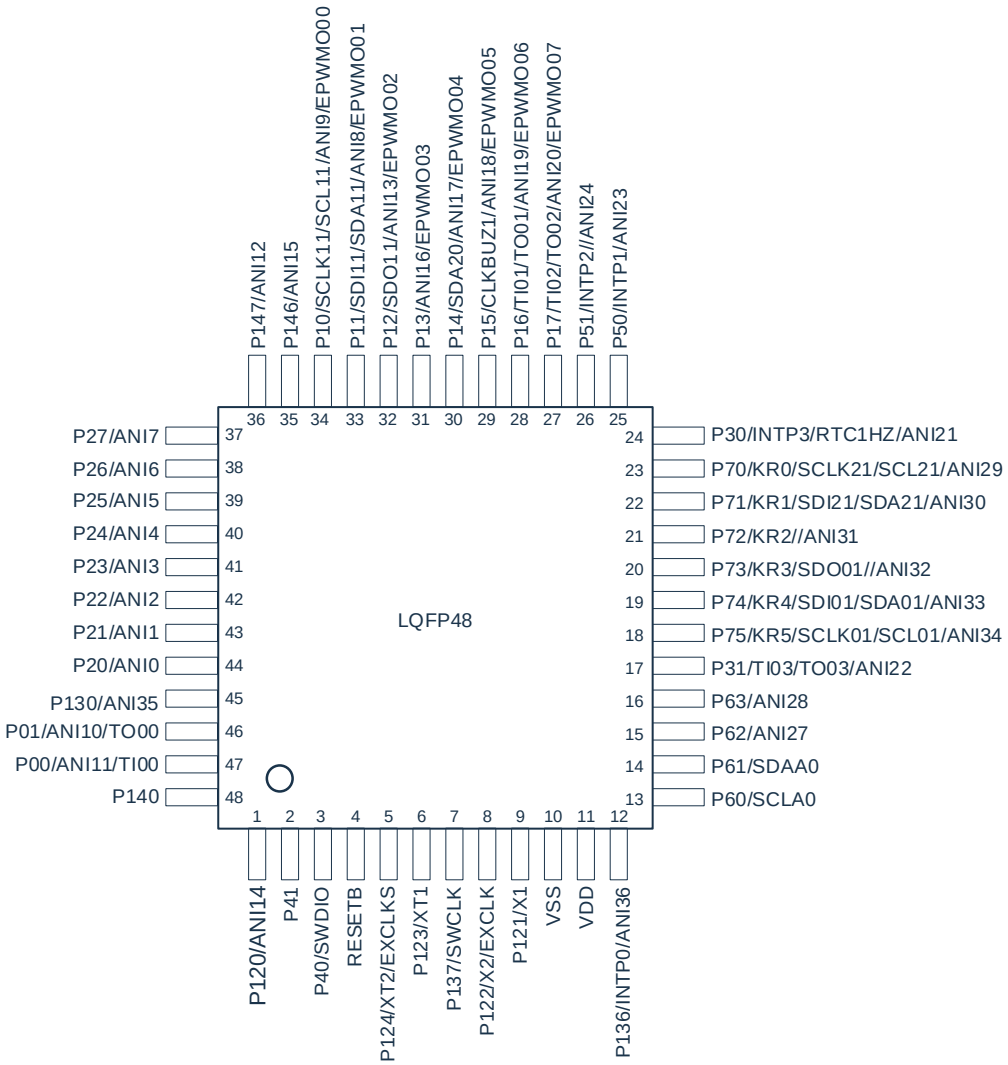
- 40-pin plastic package QFN (5x5mm, 0.4mm pitch)



Note: The unmarked digital function support pins in the figure are configurable, see section 4.1 for details.

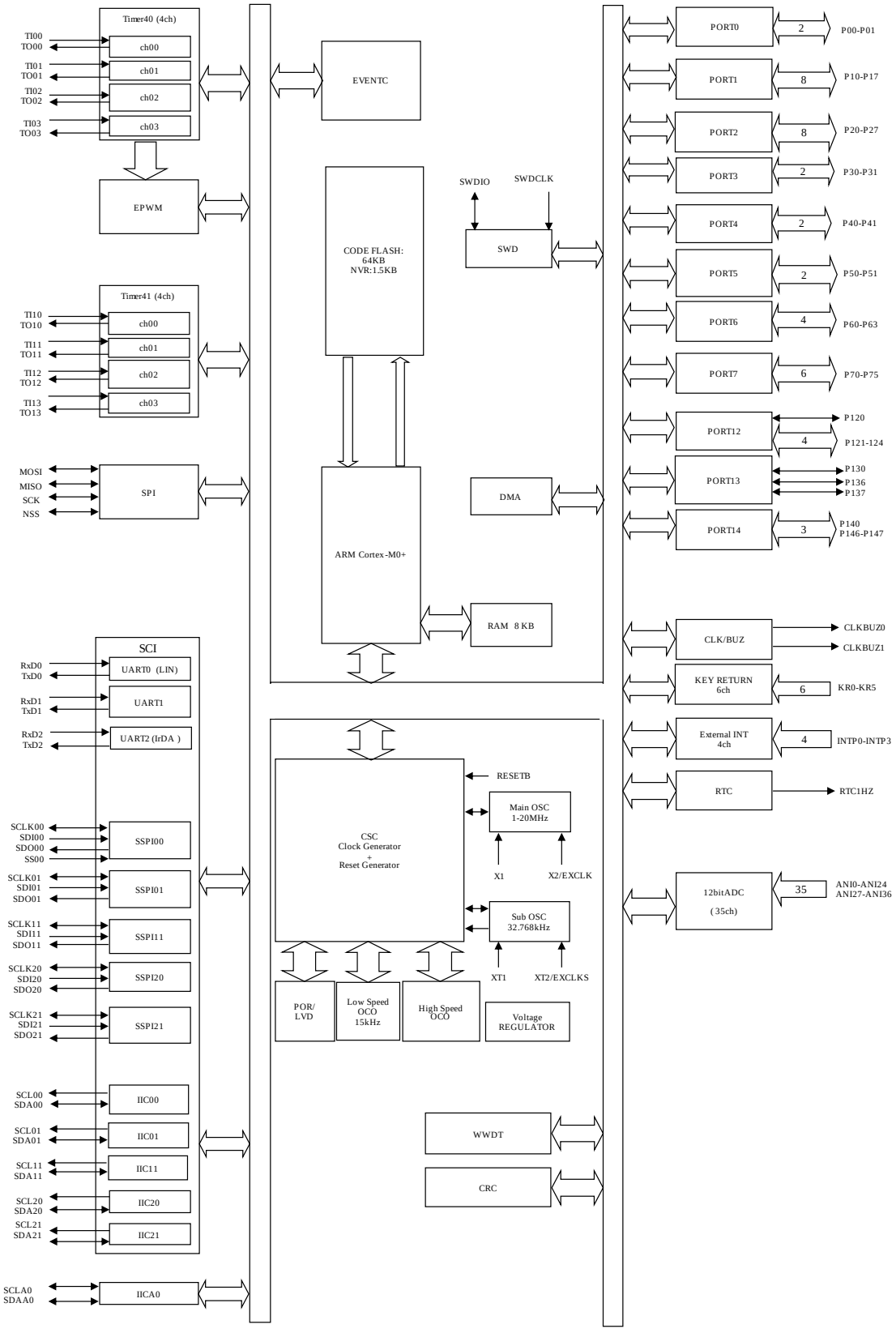
1.3.8 CMS32L051LQ48 pin diagram

- 48-pin plastic package LQFP (7x7mm, 0.5mm pitch)



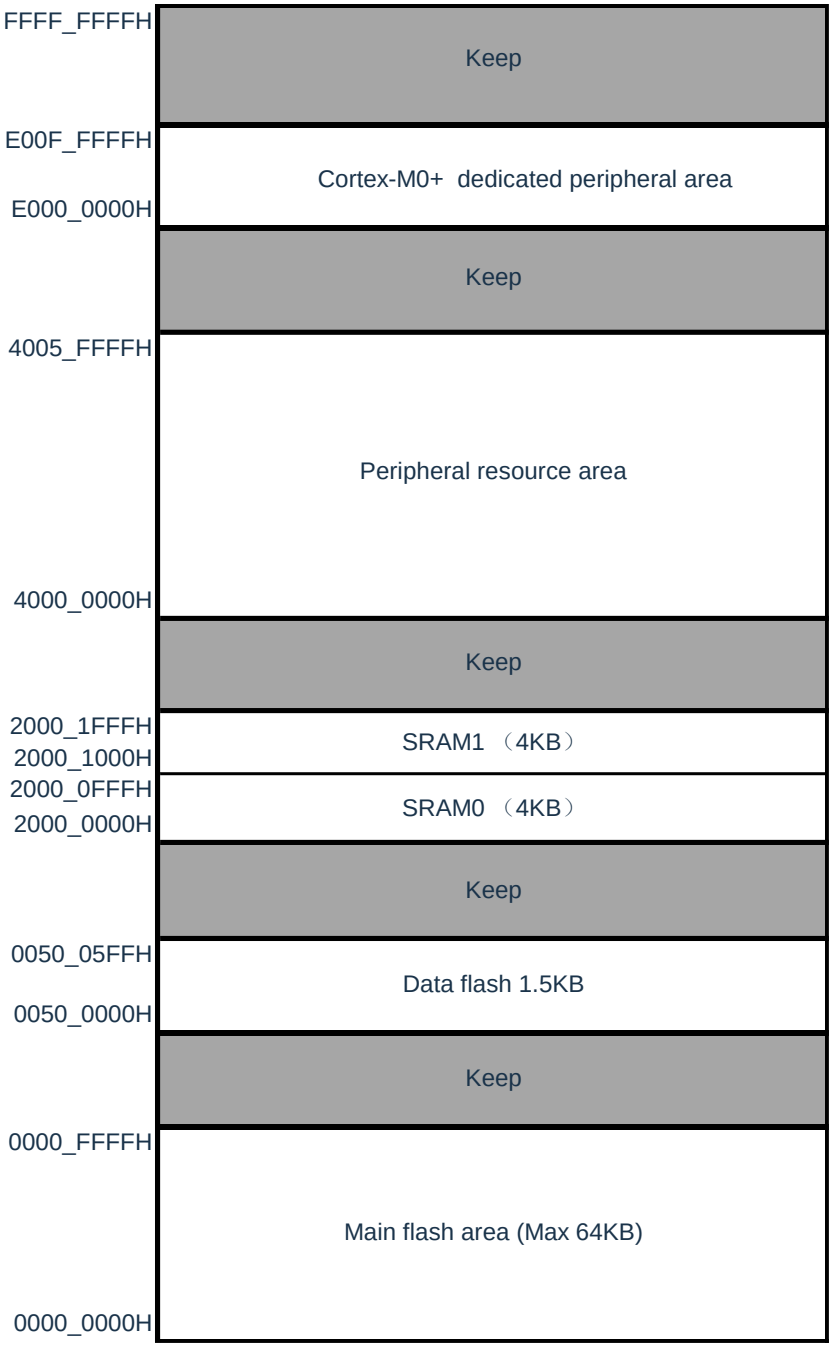
Note: The unmarked digital function support pins in the figure are configurable, see section 4.1 for details.

2 Product structure diagram



Note: The above is for 48pin product. Some functions of products below 48pin are not supported.

3 Memory mapping



4 Pin function

4.1 Port function

Table 4.1.1

Port name	Port type	Reuse function	Digital output function set register pxxcfg[3:0]	Digital input function set register xxxPCFG[5:0]	Whether the function is equipped				
					48 Pin	40 Pin	32 Pin	24 Pin	20 Pin
RESETB	Type 3	RESETB	-	-	●	●	●	●	●
P00	Type 1	GPIO	00H	00H	●	●	●		
		ANI11	00H	00H	●	●	●		
		TI00	00H	00H	●	●	●		
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●		
P01		GPIO	00H	00H	●	●	●		
		ANI10	00H	00H	●	●	●		
		TO00	00H	00H	●	●	●		
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●		
P10		GPIO	00H	00H	●	●	●	●	●
		ANI9	00H	00H	●	●	●	●	●
		SCLK11	00H	00H	●	●	●	●	●
		SCL11	00H	00H	●	●	●	●	●
		epwmo00	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P11		GPIO	00H	00H	●	●	●	●	●
		ANI8	00H	00H	●	●	●	●	●
		SDI11	00H	00H	●	●	●	●	●
		SDA11	00H	00H	●	●	●	●	●
		epwmo01	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P12		GPIO	00H	00H	●	●	●	●	●
		ANI13	00H	00H	●	●	●	●	●
		SDO11	00H	00H	●	●	●	●	●
		epwmo02	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P13		GPIO	00H	00H	●	●	●	●	●
		ANI16	00H	00H	●	●	●	●	●

		epwmo03	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P14	Type 1	GPIO	00H	00H	●	●	●	●	●
		ANI17	00H	00H	●	●	●	●	●
		SDA20	00H	00H	●	●	●	●	●
		epwmo04	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P15		GPIO	00H	00H	●	●	●	●	-
		ANI18	00H	00H	●	●	●	●	-
		CLKBUZ1	00H	00H	●	●	●	●	-
		epwmo05	00H	00H	●	●	●	●	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	-
P16		GPIO	00H	00H	●	●	●	-	-
		ANI19	00H	00H	●	●	●	-	-
		TI01	00H	00H	●	●	●	-	-
		TO01	00H	00H	●	●	●	-	-
		(SPIMOSI)	00H	00H	●	●	●	-	-
		epwmo06	00H	00H	●	●	●	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	-	-
P17		GPIO	00H	00H	●	●	●	-	-
		ANI20	00H	00H	●	●	●	-	-
		TI02	00H	00H	●	●	●	-	-
		TO02	00H	00H	●	●	●	-	-
		(SPIMISO)	00H	00H	●	●	●	-	-
		epwmo07	00H	00H	●	●	●	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	-	-
P20		GPIO	00H	00H	●	●	●	●	●
		ANI0	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P21		GPIO	00H	00H	●	●	●	●	●
		ANI1	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P22		GPIO	00H	00H	●	●	●	●	●
		ANI2	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P23		GPIO	00H	00H	●	●	●	●	●

		ANI3	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P24		GPIO	00H	00H	●	●	-	●	-
		ANI4	00H	00H	●	●	-	●	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-	●	-
P25	Type 1	GPIO	00H	00H	●	●	-	-	-
		ANI5	00H	00H	●	●	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-	-	-
P26		GPIO	00H	00H	●	-	-	-	-
		ANI6	00H	00H	●	-	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-	-	-
P27		GPIO	00H	00H	●	-	-	-	-
		ANI7	00H	00H	●	-	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-	-	-
P30		GPIO	00H	00H	●	●	●	-	-
		ANI21	00H	00H	●	●	●	-	-
		INTP3	00H	00H	●	●	●	-	-
		RTC1HZ	00H	00H	●	●	●	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	-	-
P31		GPIO	00H	00H	●	●	●	-	-
		ANI22	00H	00H	●	●	●	-	-
		TI03	00H	00H	●	●	●	-	-
		TO03	00H	00H	●	●	●	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	-	-
P40		GPIO	00H	00H	●	●	●	●	●
		SWDIO	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P41		GPIO	00H	00H	●	-	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-	-	-
P50		GPIO	00H	00H	●	●	●	-	-
		ANI23	00H	00H	●	●	●	-	-
		INTP1	00H	00H	●	●	●	-	-
		(SPINSS)	00H	00H	●	●	●	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	-	-
P51		GPIO	00H	00H	●	●	●	-	-

		ANI24	00H	00H	●	●	●	-	-
		INTP2	00H	00H	●	●	●	-	-
		(SPISCK)	00H	00H	●	●	●	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	-	-
P60		GPIO	00H	00H	●	●	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-	-	-
P61		GPIO	00H	00H	●	●	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-	-	-
P62		GPIO	00H	00H	●	-	-	-	-
	Type 1	ANI27	00H	00H	●	-	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-	-	-
P63		GPIO	00H	00H	●	-	-	-	-
		ANI28	00H	00H	●	-	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-	-	-
P70		GPIO	00H	00H	●	●	●	●	-
		ANI29	00H	00H	●	●	●	●	-
		KR0	00H	00H	●	●	-	●	-
		SCLK21	00H	00H	●	-	-	●	-
		SCL21	00H	00H	●	-	-	●	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	-
P71		GPIO	00H	00H	●	-	-	●	-
		ANI30	00H	00H	●	-	-	●	-
		KR1	00H	00H	●	-	-	●	-
		SDI21	00H	00H	●	-	-	●	-
		SDA21	00H	00H	●	-	-	●	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-	●	-
P72		GPIO	00H	00H	●	●	●	●	-
		ANI31	00H	00H	●	●	●	●	-
		KR2	00H	00H	●	●	-	●	-
		SDO21	00H	00H	●	-	-	●	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	-
P73		GPIO	00H	00H	●	●	●	●	-
		ANI32	00H	00H	●	●	●	●	-
		KR3	00H	00H	●	●	-	●	-
		SDO01	00H	00H	●	●	-	●	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	-

P74		GPIO	00H	00H	●	●	●	●	-
		ANI33	00H	00H	●	●	●	●	-
		KR4	00H	00H	●	●	-	●	-
		SDI01	00H	00H	●	●	-	●	-
		SDA01	00H	00H	●	●	-	●	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	-
P75		GPIO	00H	00H	●	●	-	●	-
		ANI34	00H	00H	●	●	-	●	-
		KR5	00H	00H	●	●	-	●	-
		SCLK01	00H	00H	●	●	-	●	-
		SCL01	00H	00H	●	●	-	●	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-	●	-
P120	Type 1	GPIO	00H	00H	●	●	●	-	-
		ANI14	00H	00H	●	●	●	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	-	-
P121	Type 2	GPIO	00H	00H	●	●	●	●	●
		X1	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P122		GPIO	00H	00H	●	●	●	●	●
		X2	00H	00H	●	●	●	●	●
		EXCLK	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P123		GPIO	00H	00H	●	●	-	-	●
		XT1	00H	00H	●	●	-	-	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-	-	●
P124		GPIO	00H	00H	●	●	-	-	●
		XT2	00H	00H	●	●	-	-	●
		EXCLKS	00H	00H	●	●	-	-	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-	-	●
P130	Type 1	GPIO	00H	00H	●	-	-	-	-
		ANI35	00H	00H	●	-	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-	-	-
P136		GPIO	00H	00H	●	●	●	-	●
		ANI36	00H	00H	●	●	●	-	●
		INTP0	00H	00H	●	●	●	-	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	-	●

P137		GPIO	00H	00H	●	●	●	●	●
		SWCLK	00H	00H	●	●	●	●	●
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	●	●
P140		GPIO	00H	00H	●	●	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-	-	-
P146		GPIO	00H	00H	●	-	-	-	-
		ANI15	00H	00H	●	-	-	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-	-	-
P147		GPIO	00H	00H	●	●	●	-	-
		ANI12	00H	00H	●	●	●	-	-
		Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●	-	-
VDD	-	Power supply	-	-	●	●	●	●	●
VSS	-	Ground	-	-	●	●	●	●	●

Note: Refer to Section 4.3 for type 1, type 2 and type 3 port type structure diagrams.

Table 4.1.2 Digital function configuration list (1/2 output function configuration)

Pin	Control register	Register configuration	Pin dual-purpose function
P00~P147	P00cfg[3:0]~P147cfg[3:0]	4'h00	Default dual-use output
		4'h01	TO10
		4'h02	TO11
		4'h03	TO12
		4'h04	TO13
		4'h05	SDO00/TxD0
		4'h06	SDO20/TxD2
		4'h07	CLKBUZ0
		4'h08	SCLKO00
		4'h09	SCLKO20
		4'h0a	TxD1

Note: P60 and P61 are NOD output, please pay attention when configuring and using.

Table 4.1.2 Digital function configuration list (2/2 input function configuration)

Control register	Register configuration	Pin dual-purpose function
TI10PCFG	6'h00	Default dual-purpose input
TI11PCFG	6'h01	P00 as a dual input
TI12PCFG	6'h02	P01 as a dual input
TI13PCFG	6'h03	P10 as a dual input
INTP0PCFG	6'h04	P11 as a dual input
INTP1PCFG	6'h05	P12 as a dual input
INTP2PCFG	6'h06	P13 as a dual input
INTP3PCFG	6'h07	P14 as a dual input
SDI00PCFG (SPI/IIC/UART)	6'h08	P15 as a dual input
SCLKI00PCFG (SPI/IIC)	6'h09	P16 as a dual input
SS00PCFG (SPI)	6'h0a	P17 as a dual input
SDI20PCFG (SPI/UART)	6'h0b	P20 as a dual input
SCLKI20PCFG (SPI)	6'h0c	P21 as a dual input
RXD1PCFG (UART)	6'h0d	P22 as a dual input
SDAA0PCFG	6'h0e	P23 as a dual input
SCLA0PCFG	6'h0f	P24 as a dual input
	6'h10	P25 as a dual input
	6'h11	P26 as a dual input
	6'h12	P27 as a dual input
	6'h13	P30 as a dual input
	6'h14	P31 as a dual input
	6'h15	P40 as a dual input
	6'h16	P41 as a dual input
	6'h17	P50 as a dual input
	6'h18	P51 as a dual input
	6'h19	P60 as a dual input

	6'h1a	P61 as a dual input
	6'h1b	P62 as a dual input
	6'h1c	P63 as a dual input
	6'h1d	P70 as a dual input
	6'h1e	P71 as a dual input
	6'h1f	P72 as a dual input
	6'h20	P73 as a dual input
	6'h21	P74 as a dual input
	6'h22	P75 as a dual input
	6'h23	P120 as a dual input
	6'h24	P121 as a dual input
	6'h25	P122 as a dual input
	6'h26	P123 as a dual input
	6'h27	P124 as a dual input
	6'h28	P130 as a dual input
	6'h29	P136 as a dual input
	6'h2a	P137 as a dual input
	6'h2b	P140 as a dual input
	6'h2c	P146 as a dual input
	6'h2d	P147 as a dual input

Table 4.1.3 SPI pin function configuration list

Register name	Register settings	SPIPin function mapping relationship			
		SPINSS	SPISCK	SPIMISO	SPIMOSI
SPIPCFG [1:0]	2'b00	Not mapped to any pins			
	2'b01	P50	P51	P17	P16
	2'b10	P63	P31	P75	P74
	1'b11	P25	P24	P23	P22

4.2 Port multiplexing function

(1/2)

Function name	input/output	Function
ANI0 ～ANI36	input	Analog input of A/D converter
INTP0 ～INTP3	input	External interrupt request input Designation of valid edges: rising edge, falling edge, rising and falling double edges
KR0 ～KR5	input	Key interrupt input
CLKBUZ0, CLKBUZ1	output	Clock output / buzzer output
RTC1HZ	output	Real-time clock correction clock (1Hz) output
RESETB	input	Low-level active system reset input. When external reset is not used, it must be connected to VDD directly or through a resistor.
IrRxD	input	IrDA serial data input
IrTxD	output	IrDA serial data output
RxD0 ～RxD2	input	Serial data input of serial interface UART0, UART1, UART2
TxD0 ～TxD2	output	Serial data output of serial interface UART0, UART1, UART2
SCL00, SCL01, SCL11, SCL20, SCL21	output	Serial clock output of serial interface IIC00, IIC01, IIC11, IIC20, IIC21
SDA00, SDA01, SDA11, SDA20, SDA21	input/ output	Serial data input/ output of serial interface IIC00, IIC01, IIC11, IIC20, IIC21
SCLK00, SCLK01, SCLK11, SCLK20, SCLK21	input/ output	Serial clock input/ output of serial interface SSPI00, SSPI01, SSPI11, SSPI20, SSPI21
SDI00, SDI01, SDI11, SDI20, SDI21	input	Serial data input of serial interface SSPI00, SSPI01, SSPI11, SSPI20, SSPI21

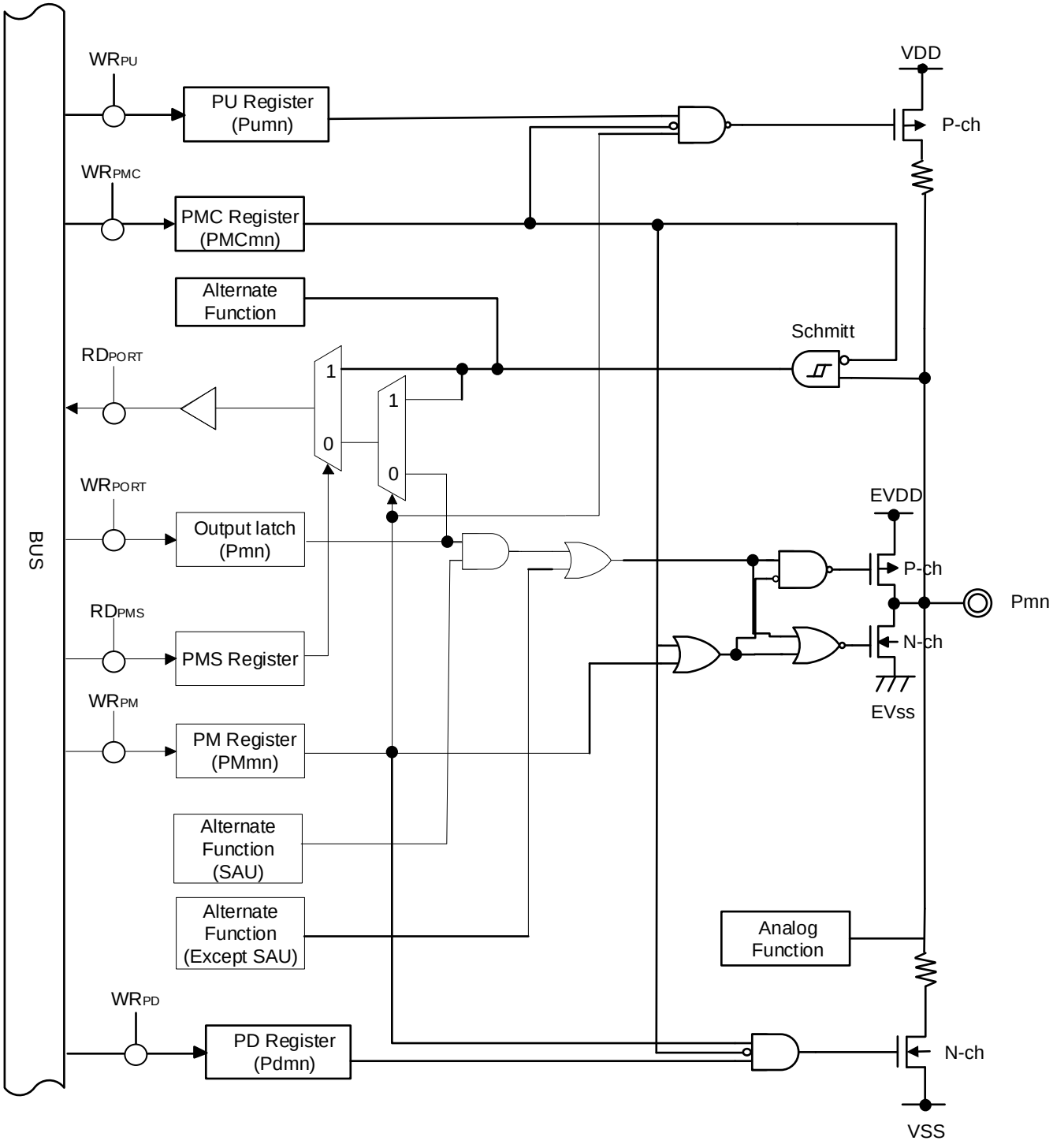
(2/2)

Function name	input/output	Function
SS00	input	Chip select input of serial interface SSPI00
SDO00, SDO01, SDO11, SDO20, SDO21	output	Serial data output of SSPI00, SSPI01, SSPI11, SSPI20, SSPI21
SPINSS	input	Chip select input of serial interface SPI
SPISCK	Input/ output	Serial clock input/output of serial interface SPI
SPIMISO	Input/ output	Serial data input/output of serial interface SPI
SPIMOSI	Input/ output	Serial data input/output of serial interface SPI
SCLA0	Input/ output	Clock input/output of serial interface IICA0
SDAA0	Input/ output	Serial data input/output of serial interface IICA0
TI00～TI03	input	16-bit timer Timer40 external count clock/capture trigger input
TO00～TO03	output	Timer output of 16-bit timer Timer40
TI10～TI13	input	16-bit timer Timer41 external count clock/capture trigger input
TO10～TO13	output	Timer output of 16-bit timer Timer41
X1, X2	—	Connect the resonator for the main system clock.
EXCLK	input	External clock input of main system clock
XT1, XT2	—	Connect the resonator for the subsystem clock.
EXCLKS	input	External clock input for subsystem clock
VDD	—	Power supply
VSS	—	Groud
SWDIO	input / output	SWD data interface
SWCLK	input	SWD clock interface

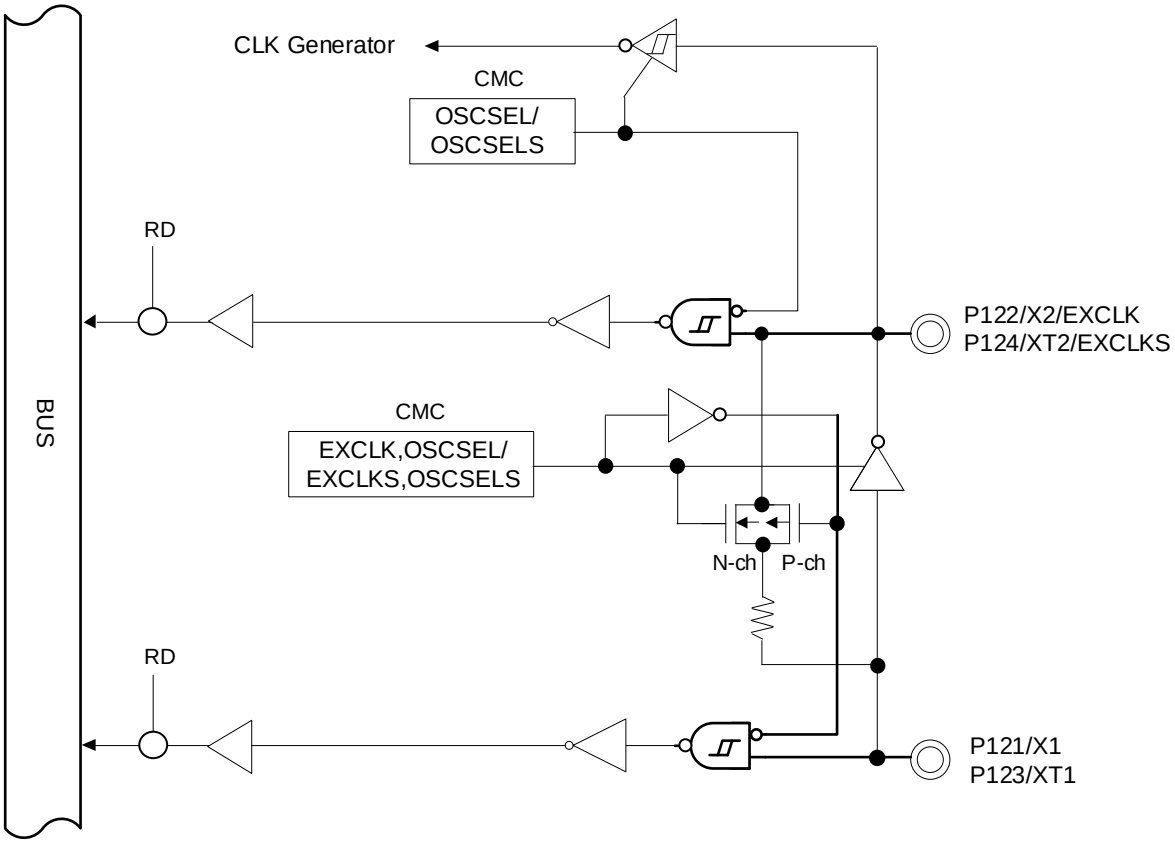
Remark: As a countermeasure for noise and locking, the bypass capacitor (about 0.1uF) must be connected with the shortest distance between VDD and VSS and thicker wiring.

4.3 Port Type

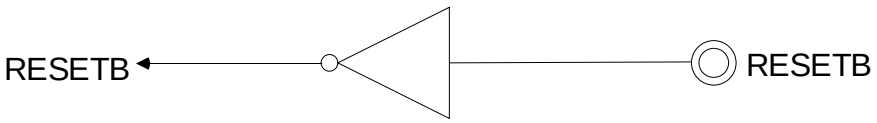
Type 1: Dual I/O function



Type 2: CLK input function



Type 3: RESET function



5 Function summary

5.1 ARM® Cortex®-M0+ core

ARM's Cortex-M0(+) processor is a new generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of a small pin count and low-power microcontroller, while providing excellent computing performance and advanced system response to interrupts.

The 32-bit RISC processor of the Cortex-M0(+) processor provides excellent code efficiency and the expected high performance of the ARM core, which is different from 8-bit and 16-bit devices of the same memory size. The Cortex-M0(+) processor has 32 address lines and a storage space of up to 4G.

CMS32L051 uses an embedded ARM core, so it is compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash

CMS32L051 has a built-in flash memory that can be programmed, erased and rewritten. Has the following functions:

- Programs and data share 64K storage space.
- 1.5KB dedicated data Flash memory
- Support page erasing, each page size is 512byte, erasing time 2ms
- Support byte/half-word/word (32bit) programming, programming time 120us

5.2.2 SRAM

CMS32L051 has built-in 8K bytes of embedded SRAM.

5.3 Enhanced DMA controller

Built-in enhanced DMA (Direct Memory Access) controller can realize the function of data transfer between memories without using CPU.

- It supports the start of DMA through peripheral function interrupts, and can realize real-time control through communication, timer and A/D.
- The transmission source/destination area is optional for the entire address space range (when the flash area is used as the destination address, the flash needs to be preset to the programming mode).
- Supports 4 transfer modes (normal transfer mode, repetitive transfer mode, block transfer mode and chain transfer mode).

5.4 Linkage controller

The linkage controller links each peripheral function output event with the peripheral function trigger source. So as to realize the coordinated operation between peripheral functions without using the CPU.

The linkage controller has the following functions:

- The event signals can be linked together to realize the linkage of peripheral functions.
- 15 types of event input, 4 types of event trigger.

5.5 Clock generation and start

The clock generation circuit is a circuit that generates a clock for the CPU and peripheral hardware. There are the following 3 types of system clocks and clock oscillation circuits.

5.5.1 Main system clock

- X1 oscillator circuit: It can generate 1-20MHz clock oscillation by connecting a resonator to the pins (X1 and X2), and can stop the oscillation by executing a deep sleep command or setting MSTOP.
- High-speed internal oscillator (high-speed OCO): The frequency can be selected for oscillation by the option byte. After the reset is released, the CPU defaults to start running with this high-speed internal oscillator clock. Oscillation can be stopped by executing a deep sleep instruction or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed internal oscillator. The highest frequency is 64Mhz, and the accuracy is ±1.0%.
- Input the external clock from the pin (X2): (1～20MHz), and the input of the external main system clock can be disabled by executing the deep sleep instruction or setting the MSTOP bit.

5.5.2 Subsystem clock

- XT1 oscillator circuit: It can generate 32.768kHz clock oscillation by connecting a 32.768kHz resonator to the pins (XT1 and XT2), and the oscillation can be stopped by setting the XTSTOP bit.
- Input the external clock from the pin (XT2): 32.768kHz, and the input of the external clock can be disabled by setting the XTSTOP bit.

5.5.3 Low-speed internal oscillator clock

Low-speed internal oscillator (low-speed OCO): generates 15kHz (TYP.) clock oscillation. The low-speed internal oscillator clock can be used as the CPU clock. The following peripheral hardware can be run by the low-speed internal oscillator clock:

- Watchdog timer（WWDT）
- Real Time Clock（RTC）
- 15-bit interval timer

5.6 Power management

5.6.1 Power supply mode

VDD: external power supply, voltage range 1.8 to 5.5V

5.6.2 Power-on reset

The power-on reset circuit (POR) has the following functions:

- An internal reset signal is generated when the power is turned on. If the power supply voltage (V_{DD}) is greater than the detection voltage (V_{POR}), the reset is released. However, before reaching the operating voltage range, the reset state must be maintained through a voltage detection circuit or an external reset.
- The power supply voltage (VDD) and the detection voltage (V_{PDR}) are compared. When $V_{DD}<V_{PDR}$, an internal reset signal is generated. However, when the power supply drops, it must be shifted to the deep sleep mode before it falls below the operating voltage range, or set to the reset state through a voltage detection circuit or an external reset. If you want to restart operation, you must confirm that the power supply voltage has returned to the operating voltage range.

5.6.3 Voltage detection

The voltage detection circuit sets the operation mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) through the option byte. The voltage detection (LVD) circuit has the following functions:

- Compare the power supply voltage (VDD) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) and generate an internal reset or interrupt request signal.
- The detection voltage of the power supply voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can select the detection level by the option byte.
- Can run in deep sleep mode.
- When the power supply rises, before reaching the operating voltage range, the reset state must be maintained through a voltage detection circuit or an external reset. When the power supply drops, it must be transferred to the deep sleep mode before being lower than the operating voltage range, or set to the reset state through a voltage detection circuit or an external reset.
- The operating voltage range varies according to the setting of the user option byte.

5.7 Low power consumption mode

CMS32L051 supports three low-power modes to achieve the best compromise between low power consumption, short startup time, and available wake-up sources:

- Sleep mode: Enter the sleep mode by executing the sleep command. The sleep mode is a mode in which the CPU operating clock is stopped. Before setting the sleep mode, if the high-speed system clock oscillator circuit, high-speed internal oscillator, or subsystem clock oscillator circuit is oscillating, each clock continues to oscillate. Although this mode cannot reduce the operating current to the level of the deep sleep mode, it is an effective mode when you want to restart processing immediately through an interrupt request or when you want to perform intermittent operation frequently.
- Deep sleep mode: Enter the deep sleep mode by executing the deep sleep command. The deep sleep mode is a mode to stop the oscillation of the high-speed system clock oscillation circuit and the high-speed internal oscillator and stop the entire system. Can greatly reduce the operating current of the chip. Because the deep sleep mode can be cancelled by an interrupt request, intermittent operation is also possible. However, in the case of the X1 clock, because it is necessary to ensure the wait time for stable oscillation when releasing the deep sleep mode, if you must start processing immediately with an interrupt request, you must select the sleep mode.

- Partial power-down deep sleep mode: Pre-configure the PMUKEY command to allow and execute the deep sleep command to enter the partial power-down deep sleep mode. The partial power-down deep sleep mode will stop RAM1 and peripherals compared with the deep sleep mode Power supply can further reduce the working current of the chip compared to the deep sleep mode. Part of the deep sleep mode that is powered down can be released by external interrupts, key-in interrupts, RTC interrupts, 15bit interval interrupts and WDT interrupt requests, so intermittent operation can also be performed

Note: 1. Before entering the deep sleep mode with partial power drop, only the shielding bits that are expected to be used to uninterrupt the sleep mode should be cleared.

2. The watchdog and low voltage detection function can only remove the deep sleep mode of partial power mode in the interrupted mode.

3. Do not use external reset, watchdog reset, or low voltage detection reset signals to remove the deep sleep mode of partial power mode.

4. When the program design needs to exit the partial power drop mode and reset the chip immediately, please first use the interrupt wake up chip, and then use the software reset instruction in the interrupt service program to achieve the chip reset operation.

In any mode except the deep sleep mode with partial power-down, the registers, flags, and data memory all retain the contents before the standby mode, and also maintain the status of the output latch and output buffer of the input/output port. It is necessary to reinitialize functions such as peripheral modules and RAM1 when the deep sleep mode with partial power failure is released.

5.8 Reset function

The following 7 methods to generate a reset signal:

1) Input external reset through RESETB pin. Note 1
2) Generate an internal reset through the program runaway detection of the watchdog timer.
3) The internal reset is generated by comparing the power supply voltage of the power-on reset (POR) circuit and the detection voltage.
4) The internal reset is generated by comparing the power supply voltage of the voltage detection circuit (LVD) and the detection voltage.
5) Internal reset due to RAM parity error.
6) Internal reset due to access to illegal memory.
7) Software reset

The internal reset is the same as the external reset. After the reset signal is generated, the program is executed from the addresses written in addresses 0000H and 0001H.

Note: 1. In deep sleep mode with partial power drop, the external reset function is prohibited.

5.9 Interrupt function

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs and 1 non-maskable interrupt (NMI) input. In addition, the processor also supports multiple internal exceptions.

This product has processed 32 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI). For details, please refer to the corresponding chapters of the user manual. The actual number of interrupt sources varies by product.

5.10 Real time clock (RTC)

The real-time clock (RTC) has the following functions.

- Counter with year, month, week, day, hour, minute and second.
- Fixed period interrupt function (period: 0.5 second, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm clock: week, hour, minute)
- 1Hz pin output function
- Support the division of the subsystem clock or the main system clock as the running clock of the RTC
- The real-time clock interrupt signal (INTRTC) can be used as a wake-up from deep sleep mode
- Support a wide range of clock correction functions

Only when the sub-system clock (32.768kHz) or the divided frequency of the main system clock is selected as the running clock of the RTC, the year, month, week, day, hour, minute and second can be counted. When the low-speed internal oscillator clock (15kHz) is selected, only the fixed cycle interrupt function can be used.

5.11 Watchdog timer

1 channel WWDT, 17bit watchdog timer is set to count operation by option byte. The watchdog timer runs on the low-speed internal oscillator clock (15kHz). The watchdog timer is used to detect program runaway. When a program out of control is detected, an internal reset signal is generated.

The following conditions are judged to be out of control of the program:

- When the watchdog timer counter overflows
- When a 1-bit operation instruction is executed on the enable register (WDTE) of the watchdog timer
- When writing data other than "ACH" to the WDTE register
- When writing data to the WDTE register while the window is closed

5.12 SysTick timer

This timer is dedicated to the real-time operating system, but it can also be used as a standard down counter.

Its characteristics are: when the 24-bit down counter self-filling capacity counter reaches 0, a maskable system interrupt is generated.

5.13 Timer timer4

This product has two built-in timer units timer4 with 4-channel 16-bit timers each 16-bit timer is called a "channel", which can be used as an independent timer or combined with multiple channels for advanced timer functions.

For details of each function, please refer to the table below:

Independent channel operation function	Multi-channel linkage operation function
● Interval timer ● Square wave output ● External event counter ● Frequency divider ● Measurement of input pulse interval ● Measurement of the high/low level width of the input signal ● Delay counter	● One-shot pulse output ● PWM output ● Multiple PWM output

5.13.1 Independent channel operation function

The independent channel operation function is a function that can independently use any channel without being affected by the operation mode of other channels. The independent channel operation function can be used in the following modes:

1) Interval timer: Can be used as a reference timer that generates interrupts (INTTM) at regular intervals.
2) Square wave output: Whenever an INTTM interrupt is generated, a flip is triggered, and a square wave with a 50% duty cycle is output from the timer output pin (TO).
3) External event counter: Count the valid edge of the input signal of the timer input pin (TI), and if it reaches the specified number of times, it can be used as an event counter to generate an interrupt.
4) Frequency divider function (only limited to channel 0 of unit 0): divide the input clock of the timer input pin (TI00), and then output from the output pin (TO00).
5) Input pulse interval measurement: start counting at the valid edge of the input pulse signal of the timer input pin (TI) and capture the count value at the valid edge of the next pulse to measure the interval of the input pulse.
6) Measurement of the high/low level width of the input signal: start counting on one edge of the input signal of the timer input pin (TI) and capture the count value on the other edge to measure the high or low level of the input signal Width.
7) Delay counter: start counting at the valid edge of the input signal of the timer input pin (TI) and generate an interrupt after any delay period has elapsed.

5.13.2 Multi-channel linkage operation function

Multi-channel linkage operation function can be realized by combining the master channel (the basic timer of the main control cycle) and the slave channel (the timer that follows the master control channel). Multi-channel linkage operation function can be used in the following modes:

1) One-shot pulse output: Use two channels in pairs to generate one-shot pulses that can set the output timing and pulse width arbitrarily.
2) PWM (Pulse Width Modulation) output: Use 2 channels in pairs to generate pulses with a period and duty cycle that can be set arbitrarily.
3) Multiple PWM (Pulse Width Modulation) output: It can generate up to 7 kinds of PWM signals with any duty cycle in a fixed cycle by expanding the PWM function and using 1 master channel and multiple slave channels.

5.13.3 8-bit timer operation function

The 8-bit timer operation function can use the 16-bit timer channel as a function of two 8-bit timer channels. (Only channel 1 and channel 3 can be used)

5.13.4 LIN-bus support function

The timer4 unit can be used to check whether the received signal in LIN-bus communication is suitable for the LIN-bus communication format.

1) Wake-up signal detection: Start counting on the falling edge of the input signal of the UART serial data input pin (RxD) and capture the count value on the rising edge to measure the low-level width. If the low-level width is greater than or equal to a certain fixed value, it is considered as a wake-up signal.
2) Interval field detection: After detecting the wake-up signal, start counting from the falling edge of the input signal of the UART serial data input pin (RxD) and capture the count value on the rising edge to measure the low-level width. If the width of the low level is greater than or equal to a certain fixed value, it is regarded as an interval field.
3) Synchronous field pulse width measurement: After detecting the interval field, measure the low-level width and high-level width of the input signal of the UART serial data input pin (RxD). Calculate the baud rate based on the bit interval of the sync field measured in this way.

5.14 EPWM output control circuit

Use Timer4's PWM output function to control one DC motor or two stepping motors.

5.15 15-bit interval timer

This product has a built-in 15-bit interval timer, which can generate interrupts (INTIT) at any time interval set in advance, and can be used to wake up from deep sleep mode.

5.16 Clock output/buzzer output control circuit

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. Clock output or buzzer output is realized by dedicated pins.

5.17 Universal serial communication unit

This product has two built-in universal serial communication units, and each unit has up to 4 serial communication channels. It can realize the communication functions of standard SPI, simple SPI, UART and simple I2C. Take the 64pin product as an example, the function allocation of each channel is as follows.

5.17.1 3-wire serial interface (simple SPI)

Synchronize data transmission and reception with the serial clock (SCK) output from the master control device.

This is a clock synchronous communication interface that uses 1 serial clock (SCK), 1 sending serial data (SO), and 1 receiving serial data (SI) to communicate with a total of 3 communication lines.

[data transmission and reception]

- 7-bit or 8-bit data length
- Phase control of sending and receiving data
- MSB/LSB priority choice

[clock control]

- Choice of master control or slave
- Phase control of input/output clock
- The transmission cycle generated by the prescaler and the internal counter of the channel
- Maximum transfer rate

Master communication: Max.f_{CLK}/2

Slave communication: Max.f_{MCK}/6

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

[Error detection flag]

- Overflow error

5.17.2 Simple SPI with slave chip select function

SPI serial communication interface supporting slave chip select input function. This is a clock synchronization that uses a slave chip select input (SSI), a serial clock (SCK), a sending serial data (SO), and a receiving serial data (SI) 4 communication lines for communication. Communication Interface.

[Data sending and receiving]

- 7-bit or 8-bit data length
- Phase control of sending and receiving data
- MSB/LSB priority choice
- Level setting of sending and receiving data

[clock control]

- Phase control of input/output clock
- The transmission cycle generated by the prescaler and the internal counter of the channel
- Maximum transfer rate

Slave communication: Max.fMCK/6

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

[Error detection flag]

- Overflow error

5.17.3 UART

The function of asynchronous communication through two lines of serial data transmission (TxD) and serial data reception (RxD). Use these two communication lines to send and receive data asynchronously (using the internal baud rate) with other communication parties according to the data frame (consisting of start bit, data, parity bit and stop bit). Full-duplex UART communication can be realized by using two channels dedicated for transmission (even-numbered channels) and dedicated for reception (odd-numbered channels), and LIN-bus can be supported by combining timer4 units and external interrupts (INTP0).

[Data sending and receiving]

- 7-bit, 8-bit or 9-bit data length
- MSB/LSB priority choice
- Selection of level setting and reverse phase of sending and receiving data
- Additional parity check bit, parity check function
- Additional stop bit, stop bit detection

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

- Error interrupt caused by framing error, parity error or overflow error

[Error detection flag]

- Frame error, parity error, overflow error

[LIN-bus function]

- Wake-up signal detection
- BF detection
- Measurement of synchronization field, calculation of baud rate

5.17.4 Simple I2C

The function of clock synchronization communication with multiple devices through two lines of serial clock (SCL) and serial data (SDA). Because this simple I2C is designed for single communication with flash memory, A/D converters and other devices, it can only be used as a master device. The start condition and stop condition are the same as the operation control register, and must comply with the AC characteristics and be processed by software.

[Data sending and receiving]

- Main control sending, main control receiving (only limited to the main control function of single main control)
- ACK output function, ACK detection function
- 8-bit data length (when sending the address, use the upper 7 bits to specify the address, and use the lowest bit for R/W control)
- Generate start and stop conditions through software

[interrupt function]

- End of transmission interrupt

[Error detection flag]

- ACK error, overflow error

[Functions not supported by simple I2C]]

- Slave sending, slave receiving
- Multi-master control function (arbitration failure detection function)
- Waiting for detection function

5.18 Standard serial peripheral interface (SPI)

The serial interface SPI has the following 2 modes:

- Operation stop mode: This is a mode used when serial transmission is not performed, which can reduce power consumption
- 3-wire serial I/O mode: This mode uses 3 lines of serial clock (SCK) and serial data bus (MISO and MOSI) to transmit 8-bit or 16-bit data with multiple devices.

5.19 Standard serial interface (IICA)

The serial interface IICA has the following 3 modes:

- Operation stop mode: This is a mode used when serial transmission is not performed, which can reduce power consumption.
- I2C bus mode (supports multiple masters): This mode uses 2 lines of serial clock (SCLA) and serial data bus (SDAA) to transmit 8-bit data with multiple devices. In line with the I2C bus format, the master device can generate "start condition", "address", "indication of the transfer direction", "data" and "stop condition" for the slave device on the serial data bus. The slave device automatically detects the received status and data through hardware. This function can simplify the I2C bus control part of the application. Because the SCLA pin and SDAA pin of the serial interface IICA are used as open-drain output, the serial clock line and the serial data bus require a pull-up resistor.
- Wake-up mode: In the deep sleep mode, when the extension code or the local station address from the autonomous control device is received, the deep sleep mode can be released by generating an interrupt request signal (INTIICA). Set through the IICA control register

5.20 Analog-to-digital converter (ADC)

This product has a built-in 12-bit resolution analog-to-digital converter SARADC, which can convert analog input to digital value and supports up to 35 channels of ADC analog input (ANI0～ANI24,ANI27～ANI36). The ADC contains the following functions:

- 12-bit resolution, conversion rate 500Ksps.
- Trigger mode: support software trigger, hardware trigger and hardware trigger in standby state
- Channel selection: support two modes of single-channel selection and multi-channel scanning
- Conversion mode: support single conversion and continuous conversion
- Working voltage: Support the working voltage range of 1.8V≤VDD≤5.5V
- It can detect the built-in reference voltage (1.45V) and temperature sensor.

ADC can set various A/D conversion modes through the following mode combinations.

Trigger mode	Software trigger	Start the conversion by software operation.
	Hardware trigger no wait mode	Start the conversion by detecting the hardware trigger.
	Hardware trigger wait mode	In the conversion standby state with the power off, the power is turned on by detecting the hardware trigger, and the conversion starts automatically after the A/D power stabilization wait time.
Channel selection mode	Select mode	Select 1 channel of analog input for A/D conversion.
	Scan mode	Perform A/D conversion on 4 channels of analog input in sequence. It is possible to select 4 consecutive channels from ANI0 to ANI15 as analog input.
Conversion mode	Single conversion mode	Perform 1 A/D conversion on the selected channel.
	Continuous conversion mode	Perform continuous A/D conversion on the selected channel until it is stopped by software.
Sampling time/conversion time	Number of sampling clocks/number of conversion clocks	The sampling time can be set by the register. The default value of the sampling clock is 4 clk, and the Min value of the conversion clock is 16 clk.

5.21 Two-wire serial debug port (SW-DP)

ARM's SW-DP interface allows to connect to the microcontroller through a serial wire debugging tool.

5.22 Security function

5.22.1 Flash CRC calculation function (high-speed CRC, general-purpose CRC)

According to different purposes and conditions of use, the following 2 CRCs can be used respectively.

- High-speed CRC: In the initialization program, it can stop the operation of the CPU and check the entire code flash area at high speed。
- General CRC: In CPU operation, it is not limited to the code flash area but can be used for multi-purpose checking.

5.22.2 RAM Parity error detection function

When reading RAM data, detect parity errors.

5.22.3 SFR protection function

Prevent the important SFR (Special Function Register) from being rewritten due to CPU runaway.

5.22.4 Illegal memory access detection function

Detect illegal access to illegal memory area (area without memory or area with restricted access).

5.22.5 Frequency detection function

Can use timer4 unit to self-check CPU or peripheral hardware clock frequency.

5.22.6 A/D test function

The A/D converter is self-tested by performing A/D conversion on the A/D analog input channel (ANI), temperature sensor output voltage, and internal reference voltage.

5.22.7 Digital output signal level detection function of input/ output port

When the input/output port is in output mode, the output level of the pin can be read.

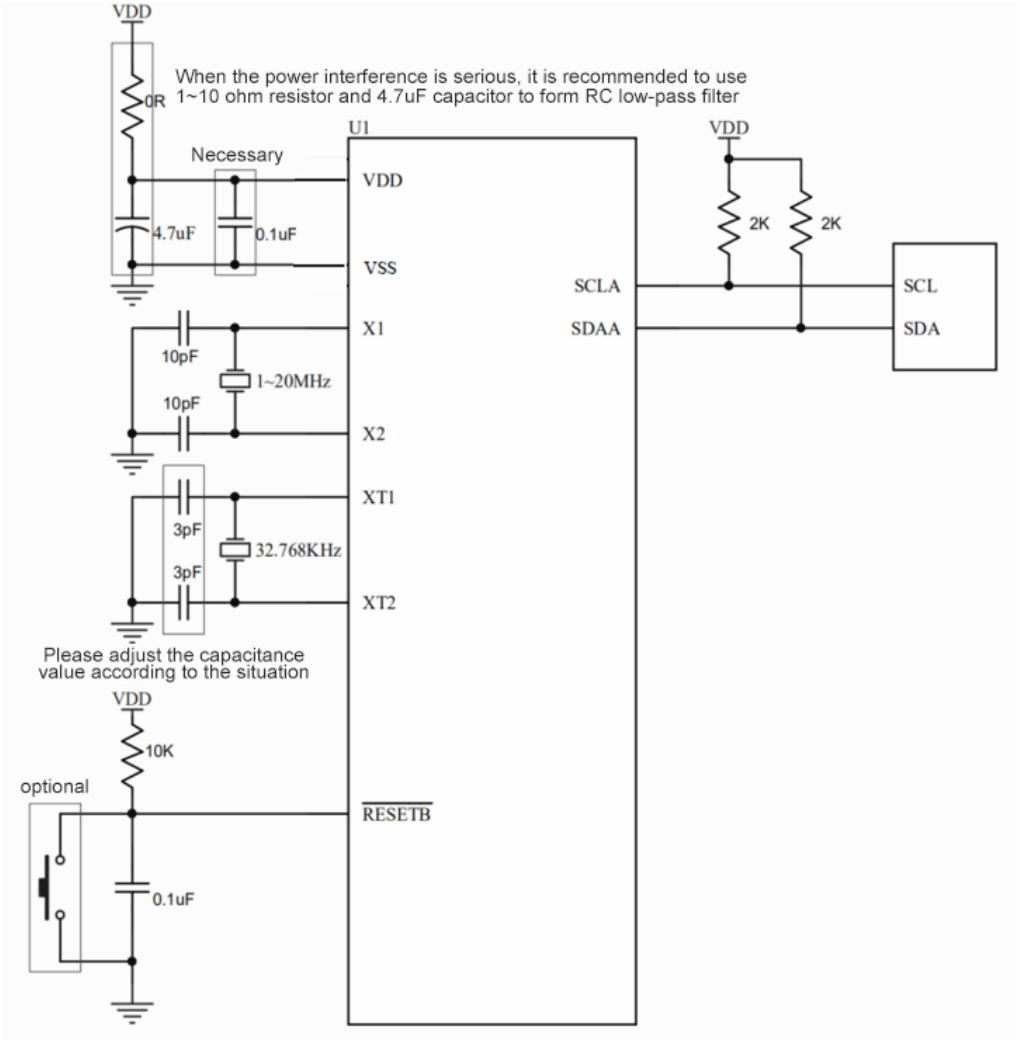
5.23 Key function

The input pin (KR0～KR4) can be interrupted by the key to generate a key interrupt (INTKR).

6 Electrical characteristics

6.1 Typical application peripheral circuit

The device connection reference of the typical MCU application peripheral circuit is as follows:



6.2 Absolute maximum voltage rating

(TA=–40～+105°C)

Item	Symbol	Condition	Rating	Unit
Source voltage	VDD		－0.5～+6.5	V
Input voltage Output voltage	VI1	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P62～P63, P70～P75, P120～P124, P130, P136, P137, P140, P146, P147, EXCLK, EXCLKS, RESETB	－0.3～VDD+0.3 note1	V
	VI2	P60～P61 (N-channel open drain)	－0.3～+6.5	V
Analog input voltage	VO	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P60～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147	－0.3～VDD+0.3 note1	V
Source voltage	VAI	ANI0～ANI24, ANI27～ANI36	－0.3～VDD+0.3note1	V

Note: 1. Do not exceed 6.5V.

2. The pin of the A/D conversion target cannot exceed AVREF (+) +0.3.

Note: Even if one of the items exceeds the absolute maximum rating for an instant, the quality of the product may be degraded. The absolute maximum rating is a rating that may cause physical damage to the product, and the product must be used under the condition that the rating is not exceeded.

Remarks:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. Use VSS as the reference voltage.

6.3 Absolute maximum current rating

(TA=–40～+105℃)

Item	Symbol	Condition		Rating	Unit
High level output current	IOH1	Each pin	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P62～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147	－40	mA
		Total pins －170mA	P00～P01, P20～P27, P40～P41, P120, P130, P136, P137, P140	－70	mA
			P10～P17, P30～P31, P50～P51, P62～P63, P70～P75, P146, P147	－100	mA
	IOH2	Each pin	P121～P124	－3	mA
		Total pins		－15	mA
Low-level output current	IOL1	Each pin	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P60～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147	40	mA
		Total pins 170mA	P00～P01, P20～P27, P40～P41, P120, P130, P136, P137, P140	100	mA
			P10～P17, P30～P31, P50～P51, P60～P63, P70～P75, P146, P147	120	mA
	IOL2	Each pin	P121～P124	15	mA
		Total pins		45	mA
Working temperature	TA	Normally run		－40～+105	℃
		When flash programming			
Storage temperature	Tstg			－65～+150	℃

Note: Even if one of the items exceeds the absolute maximum rating for an instant, the quality of the product may be degraded. The absolute maximum rating is a rating that may cause physical damage to the product, and the product must be used under the condition that the rating is not exceeded.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

6.4 Oscillation circuit characteristics

6.4.1 X1, XT1 characteristics

(TA=–40～+105℃， 1.8V≤VDD≤5.5V, VSS=0V)

item	Resonator	condition	MIN	TYP	MAX	unit
X1 clock oscillation frequency (fx)	Ceramic resonator/ crystal resonator	1.8V≤VDD≤5.5V	1.0	-	20.0	MHz
XT1 clock oscillation frequency (fxt)	Crystal resonator	1.8V≤VDD≤5.5V	32	32.768	35	kHz

Note:

1. It only indicates the allowable frequency range of the oscillation circuit. Please refer to the AC characteristics for the command execution time.
2. Please entrust the resonator manufacturer to evaluate after installing the circuit, and use it after confirming the oscillation characteristics.

6.4.2 Internal oscillator characteristics

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

resonator	condition	MIN	TYP	MAX	unit
High-speed internal oscillator clock frequency (fIH)note1,2		2.0		64.0	MHz
Clock frequency accuracy of high-speed internal oscillator	TA= - 20～+105℃	-1.0		+1.0	%
	TA= - 40～ - 20℃	-1.5note3		+1.5note3	%
Clock frequency of low-speed internal oscillator (fIL)		10	15	20	kHz

Note:

1. Select the frequency of the high-speed internal oscillator by the option byte.
2. It only shows the characteristics of the oscillation circuit, please refer to the AC characteristics for the command execution time.
3. Low temperature specification value is guaranteed by design, mass production does not measure low temperature condition.

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6.5 DC characteristics

6.5.1 Pin characteristics

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

item	symbol	condition		MIN	TYP	MAX	unit
high leveloutput Current note1	IOH1	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P62～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147 1 pin alone	1.8V≤VDD≤5.5V –40～+85℃			-12.0note2	mA
			1.8V≤VDD≤5.5V 85～+105℃			-6.0note2	
		P00～P01, P20～P27, P40～P41, P120, P130, P136, P137, P140 Total pins (when duty cycle ≤70%note3)	4.0V≤VDD≤5.5V –40～+85℃			-60.0	mA
			4.0V≤VDD≤5.5V 85～+105℃			-30.0	
			2.4V≤VDD＜4.0V			-12.0	mA
			1.8V≤VDD＜2.4V			-6.0	mA
		P10～P17, P30～P31, P50～P51, P62～P63, P70～P75, P146, P147 Total pins (when duty cycle ≤70%note3)	4.0V≤VDD≤5.5V –40～+85℃			-80.0	mA
			4.0V≤VDD≤5.5V 85～+105℃			-30.0	
			2.4V≤VDD＜4.0V			-20.0	mA
			1.8V≤VDD＜2.4V			-10.0	mA
		Total pins (when duty cycle ≤70%note3)	1.8V≤VDD≤5.5V –40～+85℃			-140.0	mA
			1.8V≤VDD≤5.5V 85～+105℃			-60.0	
	IOH2	P121 ～ P1241 pin alone	1.8V≤VDD≤5.5V			-2.5note2	mA
		Total pins (when duty cycle ≤70%note3)	1.8V≤VDD≤5.5V			-10	mA

Note:

1. This is the current value that guarantees the operation of the device even if current flows from the VDD pin to the output pin。

2. Can not exceed the total current value。

3. This is the output current value of "duty cycle≤70%condition"。

To change the output current value with a duty cycle> 70% can be calculated with the following calculation formula (when the duty cycle is changed to n%).

• The total output current of the pins = (IOH×0.7)/ (n×0.01)　　＜example＞ IOH =–10.0mA、n =80%

The total output current of the pins = (–10.0×0.7)/ (80×0.01) ≈ –8.7mA

The current of each pin does not change due to the duty cycle, and no current above the absolute maximum rating will flow.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

item	symbol	condition		MIN	TYP	MAX	unit
Low-level output current[note 1]	IOL1	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P60～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147 1 pin alone	1.8V≤VDD≤5.5V –40～+85℃			35[note2]	mA
			1.8V≤VDD≤5.5V 85～+105℃			20[note2]	
		P00～P01, P20～P27, P40～P41, P120, P130, P136, P137, P140 Total pins (when duty cycle ≤70%[note3])	4.0V≤VDD≤5.5V –40～+85℃			100	mA
			4.0V≤VDD≤5.5V 85～+105℃			70	
			2.4V≤VDD＜4.0V			30	mA
			1.8V≤VDD＜2.4V			15	mA
		P10～P17, P30～P31, P50～P51, P60～P63, P70～P75, P146, P147 Total pins (Total pins (when duty cycle ≤70%[note3])	4.0V≤VDD≤5.5V –40～+85℃			120	mA
			4.0V≤VDD≤5.5V 85～+105℃			80	
			2.4V≤VDD＜4.0V			40	mA
			1.8V≤VDD＜2.4V			20	mA
		Total pins (Total pins (when duty cycle ≤70%[note3])	1.8V≤VDD≤5.5V –40～+85℃			150	mA
			1.8V≤VDD≤5.5V 85～+105℃			100	
	IOL2	P121 ～ P124 1 pin alone	1.8V≤VDD≤5.5V			10 注2	mA
		Total pins (Total pins (when duty cycle ≤70%[note3])	1.8V≤VDD≤5.5V			40	mA

Note:

1. This is the current value that guarantees the operation of the device even if the current flows from the output pin to the VSS pin.

2. Can not exceed the total current value.

3. This is the output current value of "duty cycle≤70% condition"。

The output current value with a duty cycle> 70% can be calculated with the following calculation formula (when the duty cycle is changed to n%）

• The total output current of the pins = (IOL×0.7)/(n×0.01)

＜example＞ IOL= 10.0mA、n = 80%

The total output current of the pins = (10.0×0.7)/(80×0.01) ≈ 8.7mA

The current of each pin does not change due to the duty cycle, and no current above the absolute maximum rating will flow.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

item	symbol	condition		MIN	TYP	MAX	unit
High level input voltage	VIH1	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P62～P63, P70～P75, P120～P124, EXCLK, EXCLKS, RESETB, P130, P136, P137, P140, P146, P147	Schmidt input	0.8VDD		VDD	V
	VIH2	P60～P61		0.7VDD		6.0	V
High level input voltage	VIL1	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P62～P63, P70～P75, P120～P124, EXCLK, EXCLKS, RESETB, P130, P136, P137, P140, P146, P147	Schmidt input	0		0.2VDD	V
	VIL2	P60～P61		0		0.3VDD	V

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(TA=–40 ～ +105℃, 1.8V≤VDD≤5.5V, VSS=0V)

item	symbol	condition		MIN	TYP	MAX	unit
High level output voltage	VOH1	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P62～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147	4.0V≤VDD≤5.5V, IOH1=－12.0mA	VDD－1.5			V
			4.0V≤VDD≤5.5V, IOH1=－6.0mA	VDD－0.7			V
			2.4V≤VDD≤5.5V, IOH1=－3.0mA	VDD－0.6			V
			1.8V≤VDD≤5.5V, IOH1=－2mA	VDD－0.5			V
	VOH2	P121～P124	4.0V≤VDD≤5.5V, IOH2=－2.5mA	VDD－1.5			V
			4.0V≤VDD≤5.5V, IOH2=－1.5mA	VDD－0.7			V
			2.4V≤VDD≤5.5V, IOH2=－0.5mA	VDD－0.6			V
			1.8V≤VDD≤5.5V, IOH2=－0.4mA	VDD－0.5			V
Low-level output voltage	VOL1	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P60～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147	4.0V≤VDD≤5.5V, IOL1=35.0mA			1.2	V
			4.0V≤VDD≤5.5V, IOL1=20.0mA			0.7	V
			2.4V≤VDD≤5.5V, IOL1=9.0mA			0.4	V
			1.8V≤VDD≤5.5V, IOL1=6.0mA			0.4	V
	VOL2	P121～P124	4.0V≤VDD≤5.5V, IOL2=10.0mA			1.2	V
			4.0V≤VDD≤5.5V, IOL2=6.0mA			0.7	V
			2.4V≤VDD≤5.5V, IOL2=2.5mA			0.4	V
			1.8V≤VDD≤5.5V, IOL2=1.5mA			0.4	V

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

item	symbol	condition		MIN	TYP	MAX	unit
High-level input leakage current	ILIH1	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P60～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147	VI=VDD			1	uA
	ILIH2	RESETB	VI=VDD			1	uA
	ILIH3	P121～P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI=VDD, when input port and external clock input			1	uA
			VI=VDD, when the resonator is connected			10	uA
Low-level input leakage current	ILIL1	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P60～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147	VI=VSS			-1	uA
	ILIL2	RESETB	VI=VSS			-1	uA
	ILIL3	P121～P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI=VSS, when input port and external clock input			-1	uA
			VI=VSS, when the resonator is connected			-10	uA
Internal pull-up resistor	RU	P00～P01, P10～P17, P20～P27, P30～P31, P40～P41, P50～P51, P62～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147	VI=VSS, when input port	10	30	100	kΩ
Internal pull-down resistor	RD	P00～P01, P10～P17, P20～P27, P30～P31, P50～P51, P62～P63, P70～P75, P120, P130, P136, P137, P140, P146, P147	VI=VDD, when input port	10	30	100	kΩ

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

6.5.2 Power supply current characteristics

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

item	symbol	condition				MIN.	TYP.	MAX.	unit
Current note1	I_{DD1}	Operating mode	High-speed internal oscillator	f_{HOCO}=64MHz, f_{IH}=64MHz note3			4.5	6.9	mA
				f_{HOCO}=64MHz, f_{IH}=32MHz note3			3.5	4.5	
			High-speed main system clock	f_{MX}=20MHz note2	Input square wave		6.0	6.5	mA
					Connect the crystal		6.0	6.5	
			Subsystem clock operation	f_{SUB}=32.768kHz note4	Input square wave		175	300	uA
					Connect the crystal		175	300	
			Low-speed internal oscillator	fIL=15kHz note8			174	300	uA
	I_{DD2}	Sleep mode	High-speed internal oscillator	f_{HOCO}=64MHz, f_{IH}=64MHz note3			1.7	2.6	mA
				f_{HOCO}=32MHz, f_{IH}=32MHz note3			1.1	1.7	
			High-speed main system clock	f_{MX}=20MHz note2	Input square wave		0.85	1.3	mA
					Connecting crystal		0.85	1.3	
			Subsystem clock operation	f_{SUB}=32.768kHz note5	Input square wave		85	240	uA
					Connecting crystal		85	240	
			Low-speed internal oscillator	fIL=15kHz note8			85	240	uA
	I_{DD3} note6	Deep sleep mode note 7					80	185	uA
		Partial power-down deep sleep mode note7	T_A=–40℃~+25℃ VDD=3.0V				4.5	10	uA
			T_A=–40℃~+85℃ VDD=3.0V				4.5	80	
			T_A=–40℃~+105℃ VDD=3.0V				4.5	125	

Note:

1) This is the current flowing through VDD, including the input leakage current when the input pin is fixed to VDD or VSS. TYP. Value: CPU is in the execution of multiplication instruction (IDD1)， And does not include peripheral operating current. MAX. Value: CPU is in full instruction execution action (IDD1), and includes peripheral operating current, but does not include the flow to the A/D converter、

2) The current of the LVD circuit, I/O port, and internal pull-up or pull-down resistors does not include the current when rewriting data flash memory

3) This is the case when the high-speed internal oscillator and the subsystem clock stop oscillating.
4) This is the case where the high-speed main system clock and subsystem clock stop oscillating.
5) This is the case when the high-speed internal oscillator and the high-speed main system clock stop oscillating.
6) This is the case when the high-speed internal oscillator and the high-speed main system clock stop oscillating. Contains the current flowing to the RTC, but does not include the 15-bit interval timer and watchdog Timer current.
7) Does not include current to RTC, 15-bit interval timer and watchdog timer.
8) For the current value when the subsystem clock is running in the deep sleep mode, please refer to the current value when the subsystem clock is running in the sleep mode.
9) This is the case where the high-speed internal oscillator, the high-speed main system clock and the subsystem clock stop oscillating.

Note:

1) f_{HOCO} : The clock frequency of the high-speed internal oscillator, fIH: the system clock frequency provided by the high-speed internal oscillator。
2) f_{SUB} : External subsystem clock frequency (XT1/XT2 clock oscillation frequency).
3) f_{MX} : External main system clock frequency (X1/X2 clock oscillation frequency).
4) f_{IL} : Clock frequency of low-speed internal oscillator.
5) TYP. The temperature condition of the value is TA=25℃.

(TA=–40～+105°C, 1.8V≤VDD≤5.5V, VSS=0V)

parameter	symbol	condition	MIN.	TYP.	MAX.	Unit
Low-speed internal oscillator operating current	IFIL note1			0.2		uA
RTC operating current	IRTC note 1,2,3			0.04		uA
15-bit interval timer operating current	IIT note 1,2,4			0.02		uA
Watchdog timer operating current	IWDT note 1,2,5	fIL=15kHz		0.22		uA
A/D converter operating current	IADC note 1,6	ADC @8MHz		2.2		mA
LVD operating current	ILVD note 1,7			0.08		uA

note:

1) This is the current flowing through VDD.
2) This is the case when the high-speed internal oscillator and the high-speed system clock stop oscillating。
3) This is the current that only flows to the real-time clock (RTC) (not including the operating current of the low-speed internal oscillator and XT1 oscillator circuit). When the real-time clock is running in running mode or sleep mode, the current value of the microcontroller is IDD1 or IDD2 plus the value of IRTC. In addition, when low-speed internal oscillator is selected, IFIL must be added. IDD2 when the subsystem clock is running contains the operating current of the real-time clock.
4) This is the current that only flows to the 15-bit interval timer (not including the operating current of the low-speed internal oscillator and XT1 oscillator circuit). When the 15-bit interval timer is running in run mode or sleep mode, the current value of the microcontroller is the value of IDD1 or IDD2 plus IIT. In addition, when low-speed internal oscillator is selected, IFIL must be added.
5) This is the current that only flows to the watchdog timer (including the operating current of the low-speed internal oscillator). When the watchdog timer is running, the current value of the microcontroller is IDD1 or IDD2 or IDD3 plus the value of IWDT.
6) This is the current that only flows to the A/D converter. When the A/D converter is running in running mode or sleep mode, the current value of the microcontroller is IDD1 or IDD2 plus the value of IADC.
7) This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is the value of IDD1 or IDD2 or IDD3 plus ILVD.

Note:

1) fIL : Clock frequency of low-speed internal oscillator.
2) TYP. The temperature condition of the value is TA=25℃。

6.6 AC characteristic

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

item	symbol	condition		MIN	TYP	MAX	unit
Instruction cycle (Minimum instruction execution time)	TCY	The main system clock (f_{MAIN}) runs	1.8V≤VDD≤5.5V	0.015625		0.5	μs
		Subsystem clock (f_{SUB}) operation	1.8V≤VDD≤5.5V	28.5	30.5	31.3	μs
External system clock frequency	fEX	1.8V≤VDD≤5.5V		1.0		20.0	MHz
	fEXS	1.8V≤VDD≤5.5V		32.0		35.0	kHz
High and low level width of external system clock input	tEXH, tEXL	1.8V≤VDD≤5.5V		24			ns
	tEXHS, tEXLS	1.8V≤VDD≤5.5V		13.7			μs
TI00 ～TI03, TI10 ～TI13, input high and low level width	tTIH, tTIL	1.8V≤VDD≤5.5V		1/fMCK+10			ns
TO00 ～ TO03, TO10 ～ TO13, output frequency	fTO	4.0V≤VDD≤5.5V				16	MHz
		2.4V≤VDD＜4.0V				8	MHz
		1.8V≤VDD＜2.4V				4	MHz
CLKBUZ0, CLKBUZ1 Output frequency	fPCL	4.0V≤VDD≤5.5V				16	MHz
		2.4V≤VDD＜4.0V				8	MHz
		1.8V≤VDD＜2.4V				4	MHz
Interrupt input high and low level width	tINTH, tINTL	INTP0 ～ INTP3	1.8V≤VDD≤5.5V	1			μs
Key interrupt input high and low level width	tKR	KR0 ～ KR5	1.8V≤VDD≤5.5V	250			ns
RESETB low-level width	tRSL			10			μs

Note: f_{MCK}: Operating clock frequency of timer4 unit.

6.7 Peripheral features

6.7.1 Universal interface unit

(1) UART mode

- (T_A=–40～+85℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

item	condition		Specification Value		unit
			MIN	MAX	
Transfer rate	1.8V ≤ VDD ≤ 5.5V			f_{MCK}/6	bps
		The theoretical value of the maximum transfer rate fMCK=fCLK		10.6	Mbps

- (T_A=+85～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

item	condition		Specification Value		unit
			MIN	MAX	
Transfer rate	1.8V ≤ VDD ≤ 5.5V			fMCK/12	bps
		Theoretical value of the maximum transfer rate fMCK=fCLK		5.3	Mbps

(2) Three-wire SPImode (master mode, internal clock output)

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

item	symbol	condition		–40 ～ +85℃		+85 ～ +105℃		unit
				MIN	MAX	MIN	MAX	
SCLKp cycle time	tKCY1	tKCY1 ≥ 2/fCLK	4.0V ≤ VDD ≤ 5.5V	31.25		62.5		ns
			2.7V ≤ VDD ≤ 5.5V	41.67		83.33		
			2.4V ≤ VDD ≤ 5.5V	65		125		ns
			1.8V ≤ VDD ≤ 5.5V	125		250		ns
SCLKp high/low level width	tKH1, tKL1	4.0V ≤ VDD ≤ 5.5V		tKCY1/2–4		tKCY1/2–7		ns
		2.7V ≤ VDD ≤ 5.5V		tKCY1/2–5		tKCY1/2–10		ns
		2.4V ≤ VDD ≤ 5.5V		tKCY1/2–10		tKCY1/2–20		ns
		1.8V ≤ VDD ≤ 5.5V		tKCY1/2–19		tKCY1/2–38		ns
SDIp preparation time (to SCLKp↑)	tSIK1	4.0V ≤ VDD ≤ 5.5V		12		23		ns
		2.7V ≤ VDD ≤ 5.5V		17		33		ns
		2.4V ≤ VDD ≤ 5.5V		20		38		ns
		1.8V ≤ VDD ≤ 5.5V		28		55		ns
SDIp hold time (to SCLKp↑)	tKSI1	1.8V ≤ VDD ≤ 5.5V		5		10		ns
SCLKp↓→ SDOp output delay time	tKSO1	1.8V ≤ VDD ≤ 5.5V C=20pF note1			5		10	ns

note1.: C is the load capacitance of the SCLKp and SDOp output lines。

note: Through the port inputmode register and the port outputmode register, the SDIp pin is selected as the normal input buffer and theSDOp the pin and SCLKp pin are selected as the usual output mode.

(3) Three-wire SPImode (slave mode, external clock input)

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

item	symbol	condition		–40 ～ +85℃		+85 ～ +105℃		unit
				MIN	MAX	MIN	MAX	
SCLKp cycle time	tKCY2	4.0V ≤ VDD ≤ 5.5V	20MHz < fMCK	8/fMCK		16/fMCK		ns
			fMCK ≤20MHz	6/fMCK		12/fMCK		ns
		2.7V ≤ VDD ≤ 5.5V	16MHz < fMCK	8/fMCK		16/fMCK		ns
			fMCK ≤16MHz	6/fMCK		12/fMCK		ns
		2.4V ≤ VDD ≤ 5.5V		6/fMCK and 500		12/fMCK and 1000		ns
		1.8V ≤ VDD ≤ 5.5V		6/fMCK and 750		12/fMCK and 1500		ns
SCLKp high/low level width	tKH2, tKL2	4.0V ≤ VDD ≤ 5.5V		tKCY1/2–7		tKCY1/2–14		ns
		2.7V ≤ VDD ≤ 5.5V		tKCY1/2–8		tKCY1/2–16		ns
		1.8V ≤ VDD ≤ 5.5V		tKCY1/2–18		tKCY1/2–36		ns
SDIp preparation time (对 SCLKp↑)	tSIK2	2.7V ≤ VDD ≤ 5.5V		1/fMCK+20		1/fMCK+40		ns
		1.8V ≤ VDD ≤ 5.5V		1/fMCK+30		1/fMCK+60		ns
SDIp hold time (对 SCLKp↑)	tKSI2	1.8V ≤ VDD ≤ 5.5V		1/fMCK+31		1/fMCK+62		ns
SCLKp↓→SDOp output delay time	tKSO2	2.7V ≤ VDD ≤ 5.5V C=30pF note1			2/fMCK+44		2/fMCK+66	ns
		2.4V ≤ VDD ≤ 5.5V C=30pF note1			2/fMCK+75		2/fMCK+113	ns
		1.8V ≤ VDD ≤ 5.5V C=30pF note1			2/fMCK+100		2/fMCK+150	ns

note1: C is the load capacitance of the SCLKp and SDOp output lines.

note: Through the port inputmode register and the port outputmode register, select the SDIp pin and SCLKp pin as the normal input buffer and select the SDOp pin as the normal output mode.

(4) Four-wire SPI mode (slave mode, external clock input)

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

item	symbol	condition		–40 ～ +85℃		+85 ～ +105℃		unit
				MIN	MAX	MIN	MAX	
SSI00 set up time	tSSIK	DAPmn=0	2.7V ≤ VDD ≤ 5.5V	120		240		ns
			1.8V ≤ VDD ≤ 5.5V	200		400		ns
		DAPmn=1	2.7V ≤ VDD ≤ 5.5V	1/fMCK+120		1/fMCK+240		ns
			1.8V ≤ VDD ≤ 5.5V	1/fMCK+200		1/fMCK+400		ns
SSI00 hold time	tKSSI	DAPmn=0	2.7V ≤ VDD ≤ 5.5V	1/fMCK+120		1/fMCK+240		ns
			1.8V ≤ VDD ≤ 5.5V	1/fMCK+200		1/fMCK+400		ns
		DAPmn=1	2.7V ≤ VDD ≤ 5.5V	120		240		ns
			1.8V ≤ VDD ≤ 5.5V	200		400		ns

note: Through the port inputmode register and the port outputmode register, select the SDIp pin and SCLKp pin as the normal input buffer and select the SDOp pin as the normal outputmode.

(5) Simple IIC mode

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

item	symbol	condition	–40 ～ +85℃		+85 ～ +105℃		unit
			MIN	MAX	MIN	MAX	
SCLr Clock frequency	fSCL	2.7V ≤ VDD ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ		1000note1		400note1	kHz
		1.8V ≤ VDD ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ		400note1		100note1	kHz
		1.8V ≤ VDD ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ		300note1		75note1	kHz
Hold time when SCLr is low	t_{LOW}	2.7V ≤ VDD ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	475		1200		ns
		1.8V ≤ VDD ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ	1150		4600		ns
		1.8V ≤ VDD ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	1550		6500		ns
Hold time when SCLr is high	t_{HIGH}	2.7V ≤ VDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	475		1200		ns
		1.8V ≤ VDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1150		4600		ns
		1.8V ≤ VDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1550		6500		ns
Data establishment time (received)	$t_{SU: DAT}$	2.7V ≤ VDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK+85note2		1/fMCK+ 220note2		ns
		1.8V ≤ VDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1/fMCK+145note2		1/fMCK+ 580note2		ns
		1.8V ≤ VDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1/fMCK+230note2		1/fMCK+ 1200note2		ns
Data retention time (send)	$t_{HD: DAT}$	2.7V ≤ VDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ		305		770	ns
		1.8V ≤ VDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ		355		1420	ns
		1.8V ≤ VDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ		405		2070	ns

note: 1. Must be set to at least fMCK/4.

2. The set value of fMCK cannot exceed the holding time of SCLr="L" and SCLr="H".

6.7.2 Serial interface IICA

(1) I2C standard mode

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

item	symbol	condition	Specification Value		unit
			MIN	MAX	
SCLA0 clock frequency	fSCL	Standard mode : fCLK≥1MHz		100	kHz
Start condition set up time	tSU: STA		4.7		μs
Start condition hold time note1	tHD: STA		4.0		μs
Hold time when SCLA0 is low	tLOW		4.7		μs
Hold time when SCLA0 is high	tHIGH		4.0		μs
Data establishment time (received)	tSU: DAT		250		ns
Data retention time (send)note2	tHD: DAT		0	3.45	μs
Stop condition set up time	tSU: STO		4.0		μs
Bus idle time	tBUF		4.7		μs

note:

a) Generate the first clock pulse after generating the start condition or restarting the condition.

b) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK).

Note:

The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Standard mode: Cb=400pF, Rb=2.7kΩ

(2) I2C fast mode

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

item	symbol	condition	Specification Value		unit
			MIN	MAX	
SCLA0 clock frequency	fSCL	Fast mode: fCLK≥3.5MHz		400	kHz
Start condition set up time	tSU: STA		0.6		μs
Start condition hold time note1	tHD: STA		0.6		μs
Hold when SCLA0 is low time	tLOW		1.3		μs
Hold when SCLA0 is high time	tHIGH		0.6		μs
Data set up time (received)	tSU: DAT		100		ns
Data hold time (send)note2	tHD: DAT		0	0.9	μs
Stop condition set up time	tSU: STO		0.6		μs
Bus idle time	tBUF		1.3		μs

note:

a) Generate the first clock pulse after generating the start condition or restarting the condition.

b) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is

necessary to wait for an acknowledgement (ACK)。

Note: The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Fast mode: Cb=320pF, Rb=1.1kΩ

(3) I2C enhanced fast mode

(TA=–40～+105°C, 1.8V≤VDD≤5.5V, VSS=0V)

item	symbol	condition	Specification Value		unit
			MIN	MAX	
SCLA0 clock frequency	fSCL	Enhanced fast mode: fCLK≥10MHz		1000	kHz
Start condition set up time	tSU: STA		0.26		μs
Start condition hold time note1	tHD: STA		0.26		μs
Hold time when SCLA0 is low	tLOW		0.5		μs
When SCLA0 is high hold time	tHIGH		0.26		μs
Data set up time (received)	tSU: DAT		50		ns
Data hold time (send)note2	tHD: DAT		0	0.45	μs
Stop condition set up time	tSU: STO		0.26		μs
Bus idle time	tBUF		0.5		μs

note:

a) Generate the first clock pulse after generating the start condition or restarting the condition.

b) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK).

Note: The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Enhanced fast mode: Cb=120pF, Rb=1.1KΩ

6.8 Analog characteristic

6.8.1 A/D converter characteristic

The distinction of A/D converter characteristic

Reference voltage / Input channel	Reference voltage (+) =V_{DD} Reference voltage (–) =V_{SS}
ANI0～ANI36	Refer to the table below
Internal reference voltage, output voltage of temperature sensor	

Select the case of reference voltage (+) =V_{DD}, reference voltage (–) =V_{SS}

(T_A=–40～+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V, reference voltage (+) =V_{DD}, reference voltage (–) =V_{SS})

item	symbol	condition		MIN.	TYP.	MAX.	unit
Resolution	RES				12		bit
Composite error note 1	AINL	12-bit resolution	1.8V≤VDD≤5.5V		6		LSB
Conversion time note 3	t_{CONV}	12-bit resolution Conversion target: ANI0～ANI36	1.8V≤VDD≤5.5V	16			Tmclk
Zero error note 1	E_{ZS}	12-bit resolution	1.8V≤VDD≤5.5V		0		LSB
Full scale error note 1	E_{FS}	12-bit resolution	1.8V≤VDD≤5.5V		0		LSB
Integral linearity error note 1	ILE	12-bit resolution	1.8V≤VDD≤5.5V			±2	LSB
Differential linearity error note 1	DLE	12-bit resolution	1.8V≤VDD≤5.5V			±3	LSB
Analog input voltage	V_{AIN}	ANI0～ANI36		0		V_{DD}	V
		Internal reference voltage (1.8V≤VDD≤5.5V)		V_{BGR} note2			V
		The output voltage of the temperature sensor (1.8V≤VDD≤5.5V)		V_{TMPS25} note2			V

Note: 1. Does not include quantization error (±1/2 LSB).

2.”6.8.2 Characteristic of temperature sensor/internal reference voltage”

3. Tmclk is the AD action clock cycle, the maximum action frequency is 8MHz.

6.8.2 Characteristic of temperature sensor/internal reference voltage

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

item	symbol	condition	MIN	TYP	MAX	unit
The output voltage of the temperature sensor	VTMPS25	TA=+25℃		1.09		V
Internal reference voltage	VBGR		1.38note1	1.45	1.5note1	V
Temperature Coefficient	FVTMPS			-3.5		mV/℃
Stable operation waiting time	tAMP		5			μs

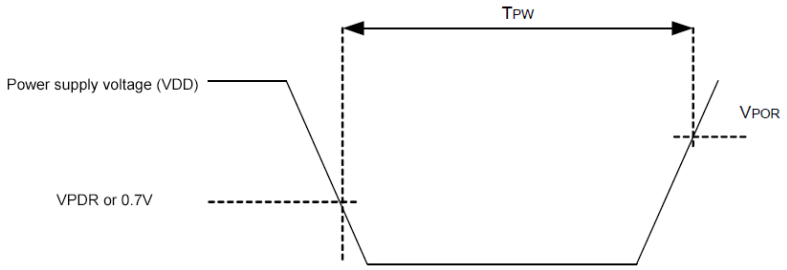
Note: Low temperature Specification Value is guaranteed by design, mass production does not measure low temperature conditions.

6.8.3 POR circuit characteristic

(TA=–40～+105℃, VSS=0V)

item	symbol	condition	MIN	TYP	MAX	unit
Detection voltage	VPOR	When the power supply voltage rises		1.50	1.75	V
	VPDR	When the power supply voltage drops	1.37	1.45		V
Minimum pulse widthnote1	TPW		300			μs

note1: This is the time required for POR to reset when VDD is lower than VPDR. In addition, in the deep sleep mode, when the main system clock (fMAIN) is stopped by setting bit0 (HIOSTOP) and bit7 (MSTOP) of the clock operation status control register (CSC), the oscillation of the main system clock (fMAIN) is stopped from VDD lower than 0.7V to rise above VPOR. Time required for POR reset.



6.8.4 LVD circuit characteristic

1) Reset mode and interrupt mode

(T_A=–40～+105℃, $V_{PDR} \leqslant V_{DD} \leqslant$5.5V, V_{SS}=0V)

item	symbol	condition	MIN	TYP	MAX	unit
Detection voltage	VLVD0	power supply voltage rises		4.06	4.14	V
		power supply voltage drops	3.90	3.98		V
	VLVD1	power supply voltage rises		3.75		V
		power supply voltage drops		3.67		V
	VLVD2	power supply voltage rises		3.13		V
		power supply voltage drops		3.06		V
	VLVD3	power supply voltage rises		3.02		V
		power supply voltage drops		2.96		V
	VLVD4	power supply voltage rises		2.92		V
		power supply voltage drops		2.86		V
	VLVD5	power supply voltage rises		2.81		V
		power supply voltage drops		2.75		V
	VLVD6	power supply voltage rises		2.71		V
		power supply voltage drops		2.65		V
	VLVD7	power supply voltage rises		2.61		V
		power supply voltage drops		2.55		V
	VLVD8	power supply voltage rises		2.50		V
		power supply voltage drops		2.45		V
	VLVD9	power supply voltage rises		2.09		V
		power supply voltage drops		2.04		V
	VLVD10	power supply voltage rises		1.98		V
		power supply voltage drops		1.94		V
	VLVD11	power supply voltage rises		1.88	1.91	V
		power supply voltage drops	1.80	1.84		V
Minimum pulse width	tLW		300			μs
Detection delay					300	μs

2) 中断和复位模式

(T_A=–40～+105℃, V_{PDR} ≤V_{DD}≤5.5V, V_{SS}=0V)

item	symbol	condition			MIN.	TYP.	MAX.	unit
Interrupt & reset mode	V_{LVDA0}	V_{POC2}，V_{POC1}，V_{POC0}=0，0，0,下降复位电压			1.60	1.63		V
	V_{LVDA1}		LVIS1，LVIS0=1，0	rising reset release voltage		1.77	1.81	V
				drop interrupt voltage	1.70	1.73		V
	V_{LVDA2}		LVIS1，LVIS0=0，1	rising reset release voltage		1.88		V
				drop interrupt voltage		1.84		V
	V_{LVDA3}		LVIS1，LVIS0=0，0	rising reset release voltage		2.92		V
				drop interrupt voltage		2.86		V
	V_{LVDB0}	V_{POC2}，V_{POC1}，V_{POC0}=0，0，1, decrease reset voltage				1.84		V
	V_{LVDB1}		LVIS1，LVIS0=1，0	rising reset release voltage		1.98		V
				drop interrupt voltage		1.94		V
	V_{LVDB2}		LVIS1，LVIS0=0，1	rising reset release voltage		2.09		V
				drop interrupt voltage		2.04		V
	V_{LVDB3}		LVIS1，LVIS0=0，0	rising reset release voltage		3.13		V
				drop interrupt voltage		3.06		V
	V_{LVDC0}	V_{POC2}，V_{POC1}，V_{POC0}=0，1，0, decrease reset voltage				2.45		V
	V_{LVDC1}		LVIS1，LVIS0=1，0	rising reset release voltage		2.61		V
				drop interrupt voltage		2.55		V
	V_{LVDC2}		LVIS1，LVIS0=0，1	rising reset release voltage		2.71		V
				drop interrupt voltage		2.65		V
	V_{LVDC3}		LVIS1，LVIS0=0，0	rising reset release voltage		3.75		V
				drop interrupt voltage		3.67		V
	V_{LVDD0}	V_{POC2}，V_{POC1}，V_{POC0}=0，1，1, decrease reset voltage				2.75		V
	V_{LVDD1}		LVIS1，LVIS0=1，0	rising reset release voltage		2.92		V
				drop interrupt voltage		2.86		V
	V_{LVDD2}		LVIS1，LVIS0=0，1	rising reset release voltage		3.02		V
				drop interrupt voltage		2.96		V
	V_{LVDD3}		LVIS1，LVIS0=0，0	rising reset release voltage		4.06	4.14	V
				drop interrupt voltage	3.90	3.98		V

6.8.5 Reset time and rising slope of the power supply voltage

(TA=–40～+105℃, VSS=0V)

item	symbol	condition	MIN	TYP	MAX	unit
Reset time	T_{RESET}			1		Ms
The rising slope of the power supply voltage	SVDD				54	V/ms

6.9 Memory characteristic

6.9.1 Flash Memory

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

Symbol	Parameter	Conditions	MIN	MAX	Unit
Tprog	Word Program (32bit)	Ta=–40～+105℃		120	μs
Terase	Sector erase (512B)	Ta=–40～+105℃	2	3	ms
	Chip erase	Ta=–40～+105℃	30	40	ms
N_{END}	Endurance	Ta=–40～+105℃	100		kcycle
t_{RET}	Data retention	100 kcycle (note2) at Ta = 105℃	20		Years

Note1: Data based on characterization results, not tested in production.

Note2: Cycling performed over the whole temperature range.

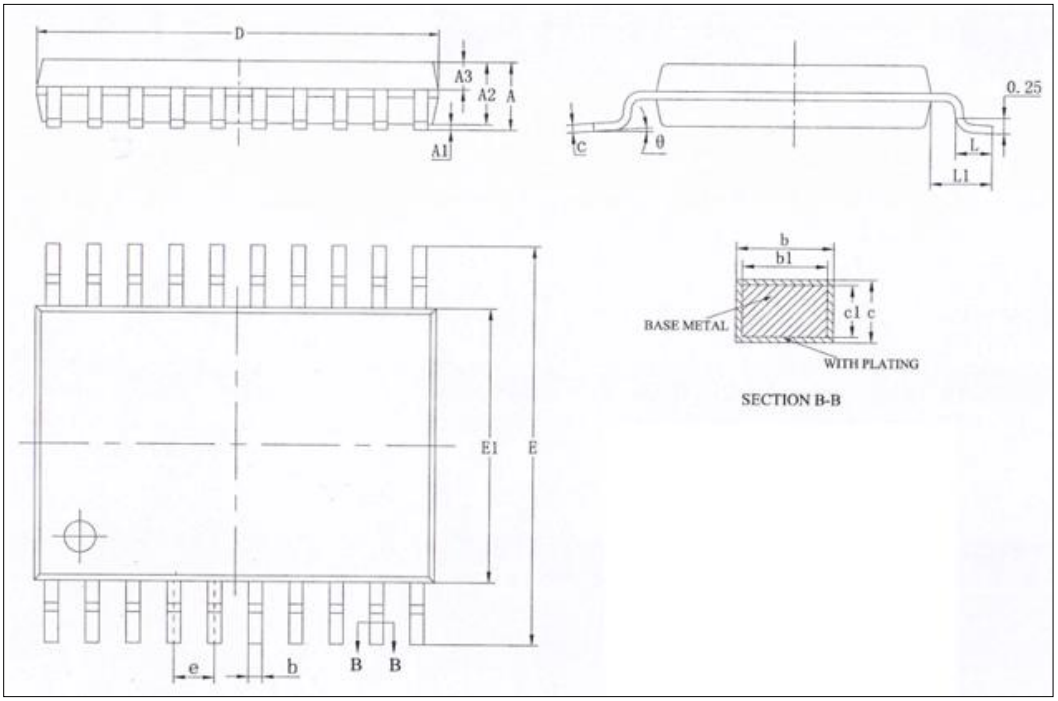
6.9.2 RAM Memory

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

Symbol	Parameter	Conditions	MIN	MAX	Unit
$V_{ramhold}$	RAM Hold Voltage	Ta=–40～+105℃	0.8		V

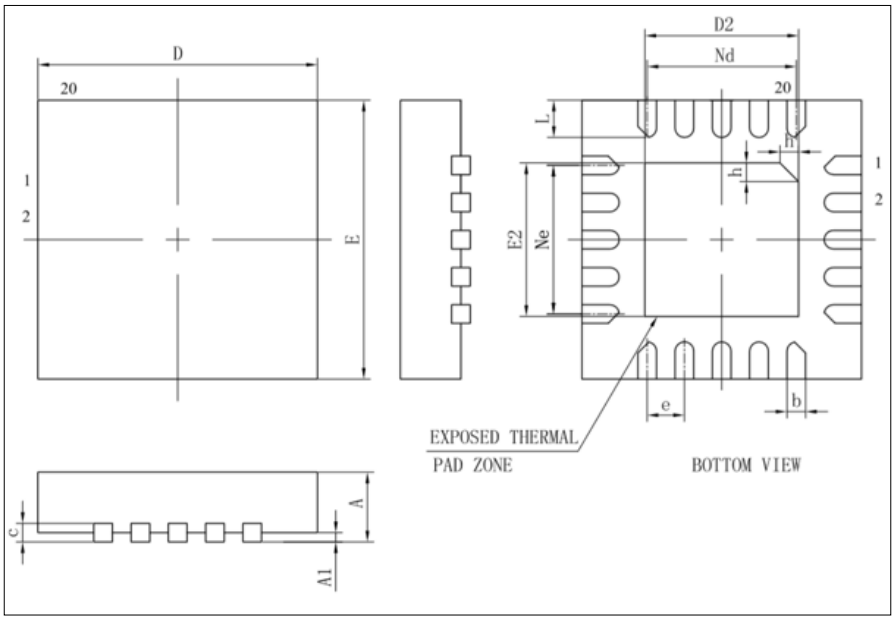
7 Package size chart

7.1 TSSOP20 (6.5x4.4mm，0.65mm spacing)



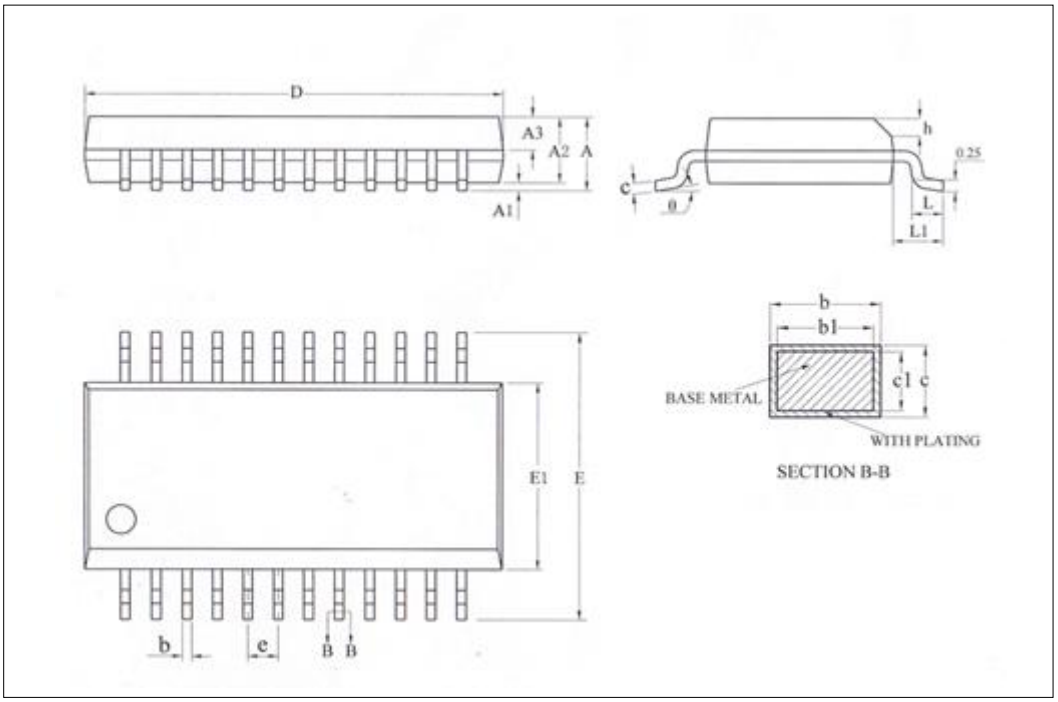
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

7.2 QFN20 (3x3mm，0.4mm spacing)



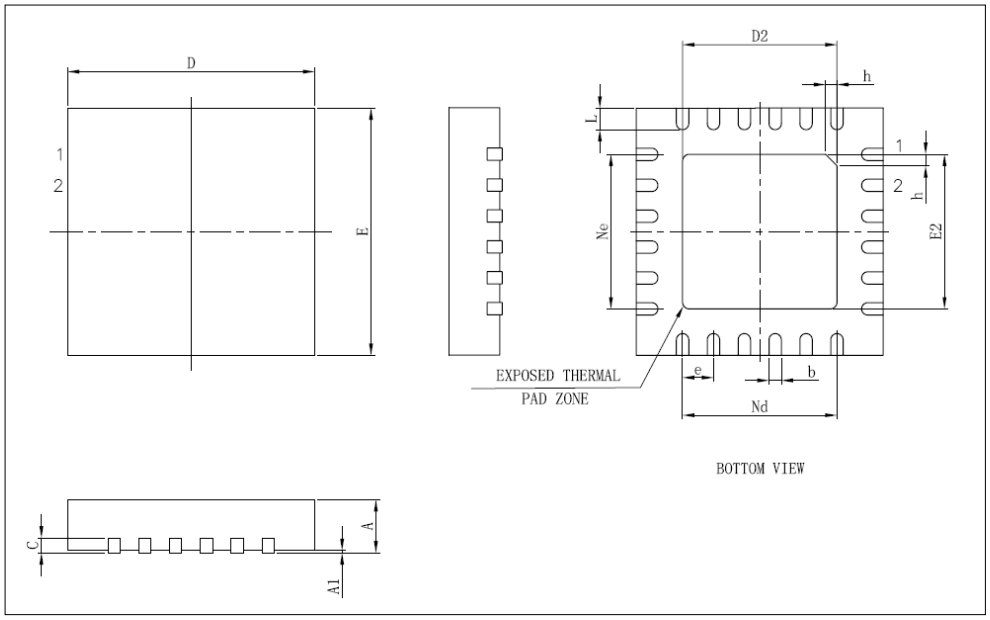
Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30

7.3 SSOP24 (8.65x3.9mm，0.635mm spacing)



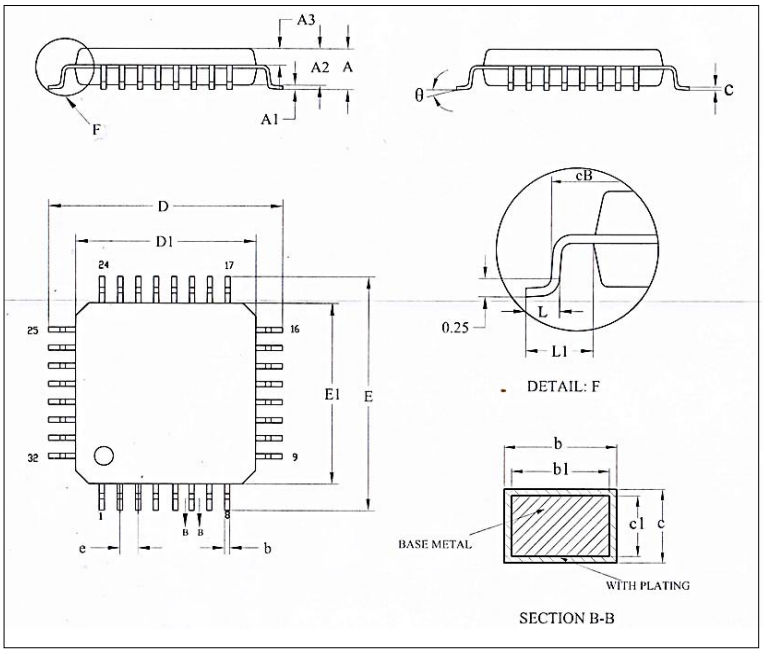
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.25
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E1	3.80	3.90	4.00
E	5.80	6.00	6.20
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

7.4 QFN24 (4x4mm，0.5mm spacing)



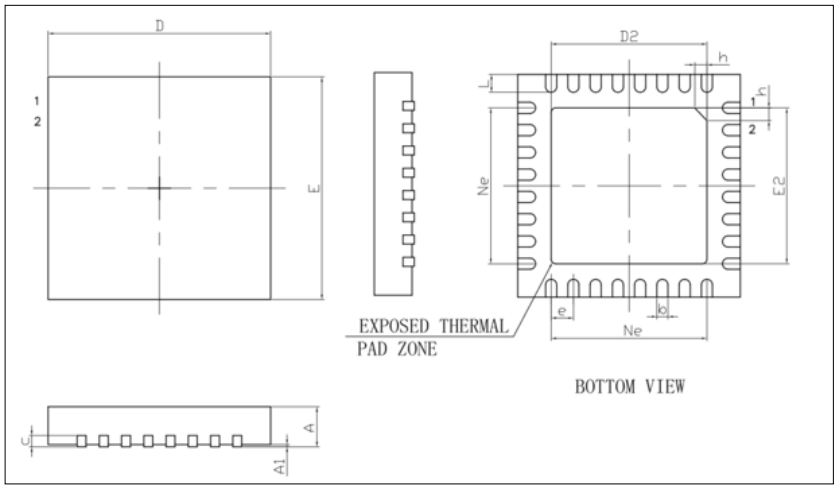
Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

7.5 LQFP32 (7x7mm,0.8mm spacing)



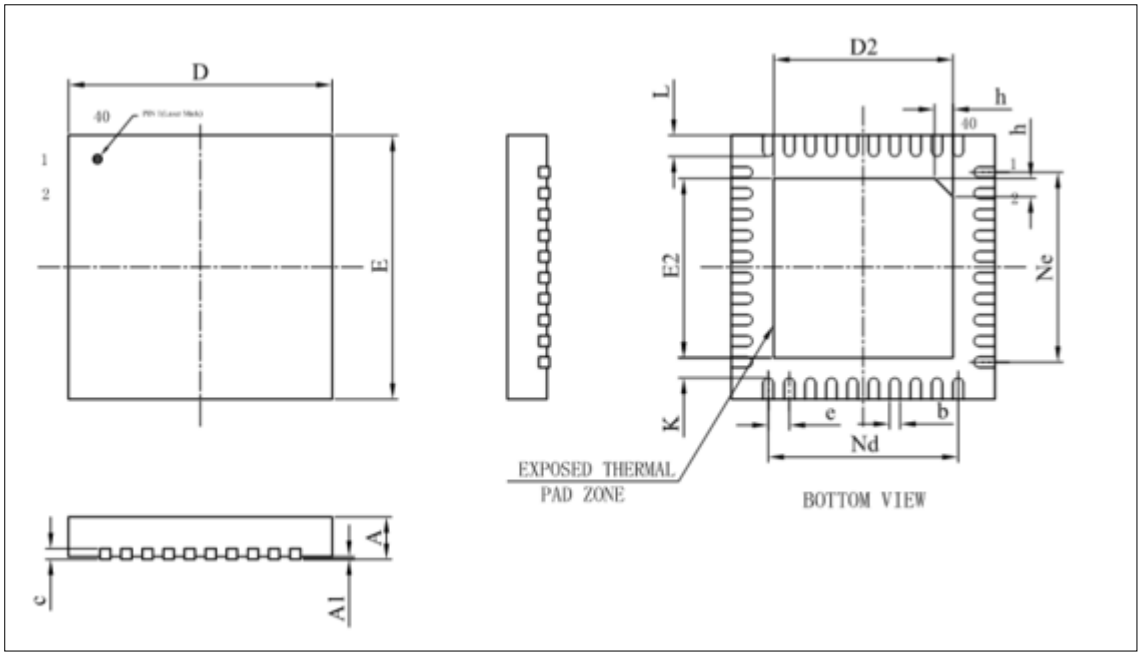
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.41
b1	0.32	0.35	0.38
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

7.6 QFN32（5x5mm, 0.5mm spacing）



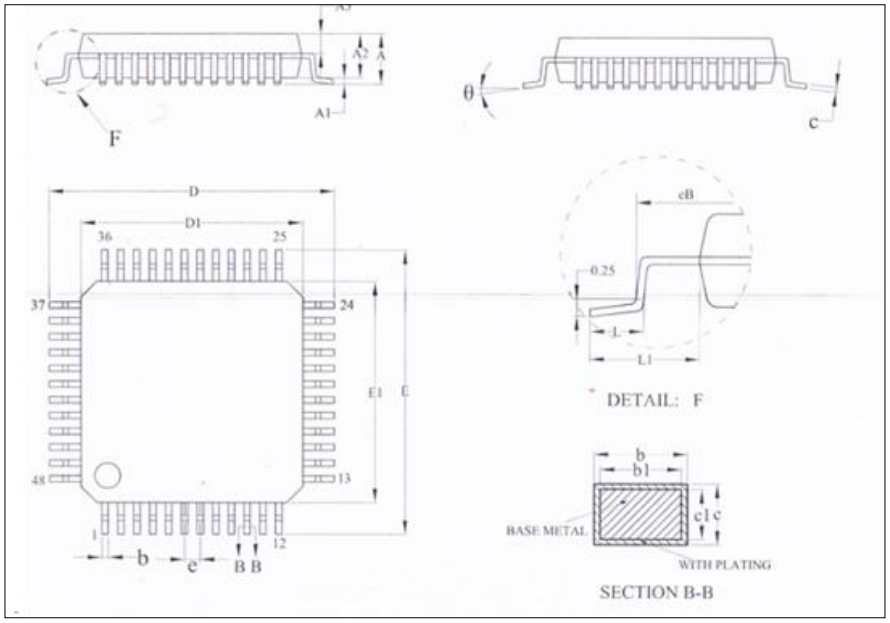
Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

7.7 QFN40 (5x5mm,0.4mm spacing)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	-	-
h	0.30	0.35	0.40

7.8 LQFP48 (7x7mm,0.5mm spacing)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

8 Revision History

Revision	Date	Modify content	
		Page/section	content
1.00	2021.05.10	—	Original Issue
1.10	2021.08.17	6.5.2	Misrepresentation
1.20	2021.09.08	1.3, 7.1-7.3	Add package types – TSSOP20
1.30	2021.10.29	1.3, 7.1-7.3	Add package types – SSOP24
1.40	2021.11.10	1.3, 7.1-7.3	Add package types – QFN32
1.50	2021.12.20	6.5.2	Modify the power supply current characteristics
1.60	2022.03.03	1.3.2, 7.2	Add package types – QFN24
1.70	2022.06.10	4.1, 4.3 5.7, 5.8	Add port function and type Add note for Low power consumption mode
1.80	2022.08.26	1.3, 7	Adjust pin diagram